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MS-7543 ATX Version: 0B

CPU: BloomField Processors In LGA1366 Package.

System Chipset:

Intel Tylersburg I/O Hub 36S (North Bridge)
Intel ICH10R (South Bridge)

On Board Devices:

CLOCK Gen -- ICS 9LPRS113
LPC Super I/O -- Fintek F71882F
Dual LAN --BCM5784M
HD Audio Codec -- ALC888S
1394 Controller -- TI TSB43AB22A
ODD_SATA /IDE -- JMB363
eSATA -- SIL3123

Main Memory:


3-Channel A / B / C DDR-III *3

Expansion Slots:

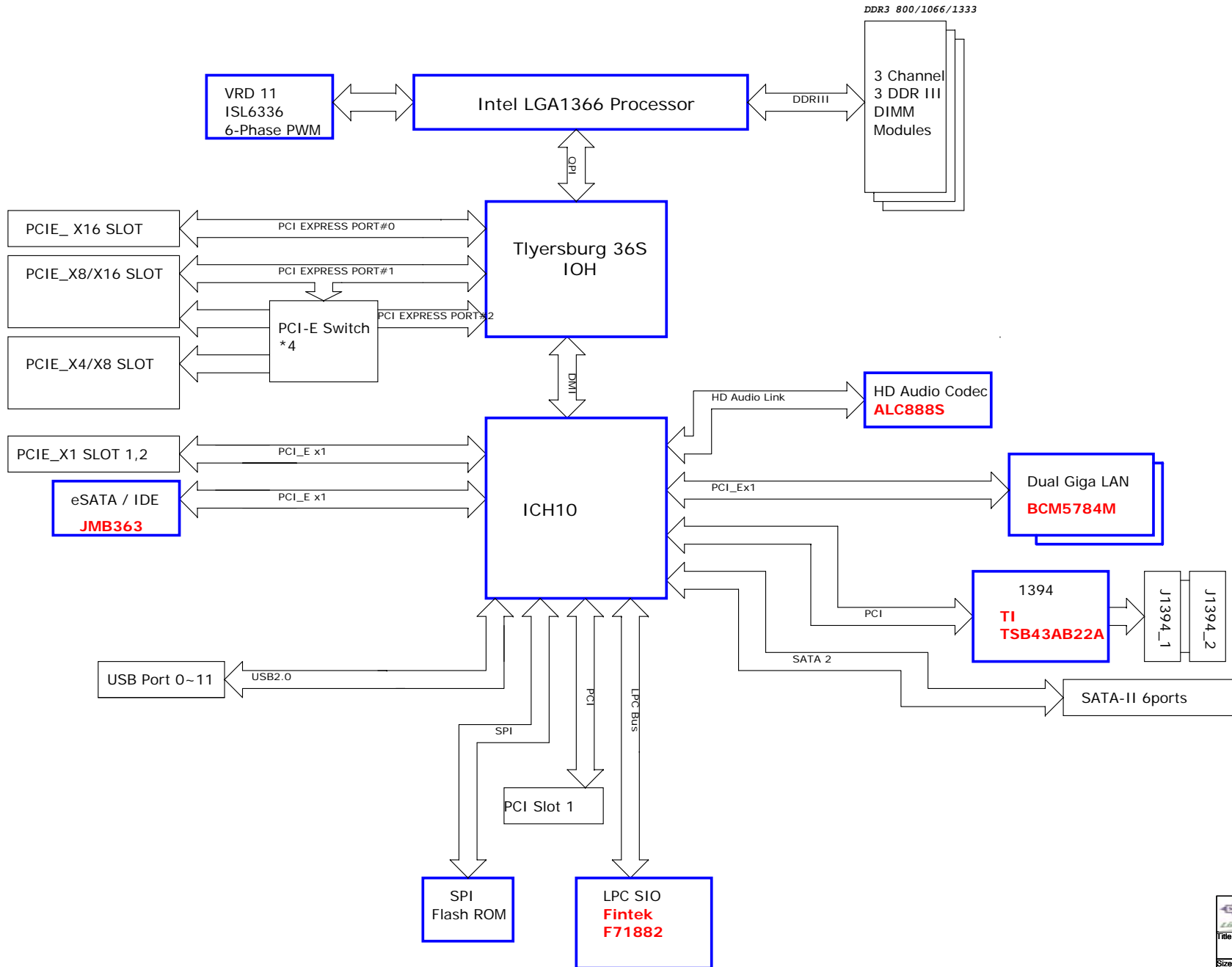
PCI EXPRESS X16 SLOT *3
PCI EXPRESS X1 SLOT * 2
PCI SLOT * 1

PWM: VR11.1 Intersil ISL6336 (6 Phases)

DELL Suzuka MLK

 MICRO-START INT'L CO.,LTD.		
Title COVER SHEET		
Size	Document Number	Rev
Custom	DELL Suzuka MLK (MS-7543)	0B
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Block Diagram



9 DATA_A[0..63] <<>

10 DATA_B[0..63] <<>

11 DATA_C[0..63] <<>

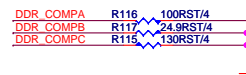
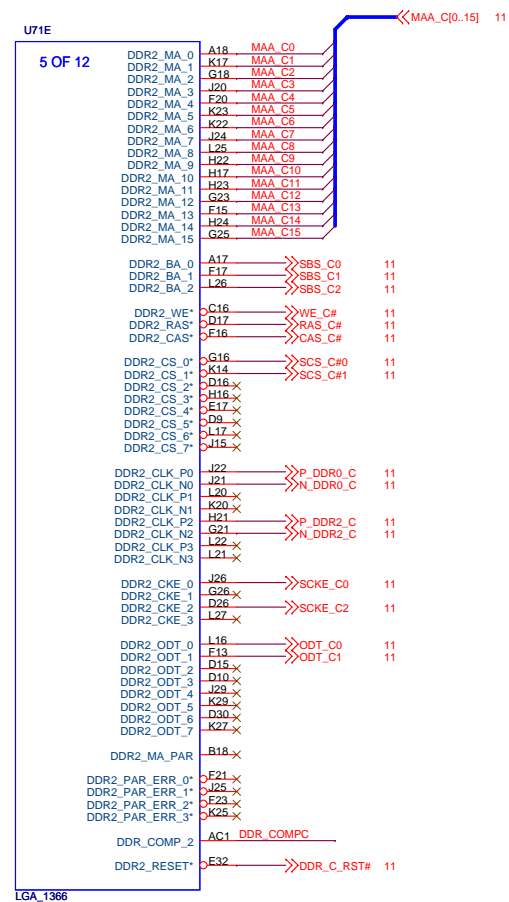
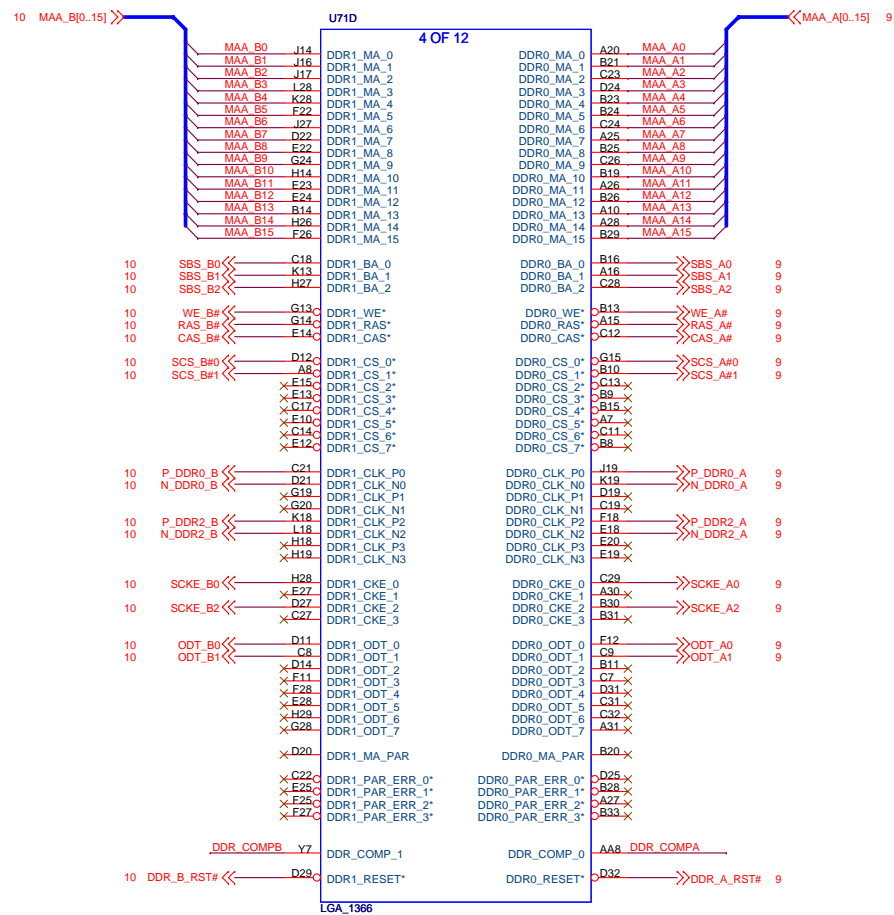
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DATA A0	W41	DDR0_DQ_0	DDR0_DQS_P0	T43	QDS_A0	9			
DATA A1	V41	DDR0_DQ_1	DDR0_DQS_N0	U43	QDS_A#0	9			
DATA A2	R43	DDR0_DQ_2		L41	QDS_A1	9			
DATA A3	R42	DDR0_DQ_3	DDR0_DQS_P1	M41	QDS_A#1	9			
DATA A4	W40	DDR0_DQ_4	DDR0_DQS_N1						
DATA A5	W42	DDR0_DQ_5		F41	QDS_A2	9			
DATA A6	U41	DDR0_DQ_6	DDR0_DQS_P2	G41	QDS_A#2	9			
DATA A7	T42	DDR0_DQ_7	DDR0_DQS_N2						
DATA A8	N41	DDR0_DQ_8		B39	QDS_A3	9			
DATA A9	N43	DDR0_DQ_9	DDR0_DQS_P3	B40	QDS_A#3	9			
DATA A10	K42	DDR0_DQ_10	DDR0_DQS_N3						
DATA A11	K43	DDR0_DQ_11		E3	QDS_A4	9			
DATA A12	P42	DDR0_DQ_12	DDR0_DQS_P4	E4	QDS_A#4	9			
DATA A13	P41	DDR0_DQ_13	DDR0_DQS_N4						
DATA A14	L42	DDR0_DQ_14		K2	QDS_A5	9			
DATA A15	L43	DDR0_DQ_15	DDR0_DQS_P5	K3	QDS_A#5	9			
DATA A16	H41	DDR0_DQ_16	DDR0_DQS_N5						
DATA A17	H43	DDR0_DQ_17		R2	QDS_A6	9			
DATA A18	E42	DDR0_DQ_18	DDR0_DQS_P6	R3	QDS_A#6	9			
DATA A19	E43	DDR0_DQ_19	DDR0_DQS_N6						
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DATA A21	J41	DDR0_DQ_21	DDR0_DQS_P7	W1	QDS_A#7	9			
DATA A22	F43	DDR0_DQ_22	DDR0_DQS_N7						
DATA A23	F42	DDR0_DQ_23		D34					
DATA A24	D40	DDR0_DQ_24	DDR0_DQS_P8	D35					
DATA A25	C41	DDR0_DQ_25	DDR0_DQS_N8						
DATA A26	A38	DDR0_DQ_26		V43					
DATA A27	D37	DDR0_DQ_27	DDR0_DQS_P9	V42					
DATA A28	D41	DDR0_DQ_28	DDR0_DQS_N9						
DATA A29	D42	DDR0_DQ_29		N42					
DATA A30	C38	DDR0_DQ_30	DDR0_DQS_P10	M43					
DATA A31	B38	DDR0_DQ_31	DDR0_DQS_N10						
DATA A32	B5	DDR0_DQ_32		H42					
DATA A33	C4	DDR0_DQ_33	DDR0_DQS_P11	G43					
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DATA A35	G3	DDR0_DQ_35		D39					
DATA A36	B6	DDR0_DQ_36	DDR0_DQS_P12	C39					
DATA A37	C6	DDR0_DQ_37	DDR0_DQS_N12						
DATA A38	F3	DDR0_DQ_38		D5					
DATA A39	F2	DDR0_DQ_39	DDR0_DQS_P13	D4					
DATA A40	H2	DDR0_DQ_40	DDR0_DQS_N13						
DATA A41	H1	DDR0_DQ_41		J2					
DATA A42	L1	DDR0_DQ_42	DDR0_DQS_P14	J1					
DATA A43	M1	DDR0_DQ_43	DDR0_DQS_N14						
DATA A44	G1	DDR0_DQ_44		P2					
DATA A45	H3	DDR0_DQ_45	DDR0_DQS_P15	P1					
DATA A46	L3	DDR0_DQ_46	DDR0_DQS_N15						
DATA A47	L2	DDR0_DQ_47		V2					
DATA A48	N1	DDR0_DQ_48	DDR0_DQS_P16	V3					
DATA A49	N2	DDR0_DQ_49	DDR0_DQS_N16						
DATA A50	T1	DDR0_DQ_50		B36					
DATA A51	T2	DDR0_DQ_51	DDR0_DQS_P17	B35					
DATA A52	M3	DDR0_DQ_52	DDR0_DQS_N17						
DATA A53	N3	DDR0_DQ_53							
DATA A54	R4	DDR0_DQ_54							
DATA A55	T3	DDR0_DQ_55							
DATA A56	U4	DDR0_DQ_56							
DATA A57	Y1	DDR0_DQ_57							
DATA A58	Y2	DDR0_DQ_58							
DATA A59	Y3	DDR0_DQ_59							
DATA A60	U1	DDR0_DQ_60							
DATA A61	U3	DDR0_DQ_61							
DATA A62	V4	DDR0_DQ_62							
DATA A63	W4	DDR0_DQ_63							
C36		DDR0_ECC_0							
A36		DDR0_ECC_1							
F32		DDR0_ECC_2							
C33		DDR0_ECC_3							
C37		DDR0_ECC_4							
A37		DDR0_ECC_5							
B34		DDR0_ECC_6							
C34		DDR0_ECC_7							

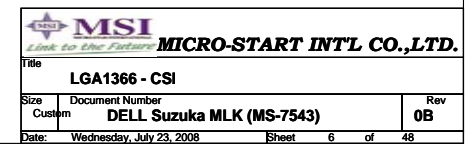
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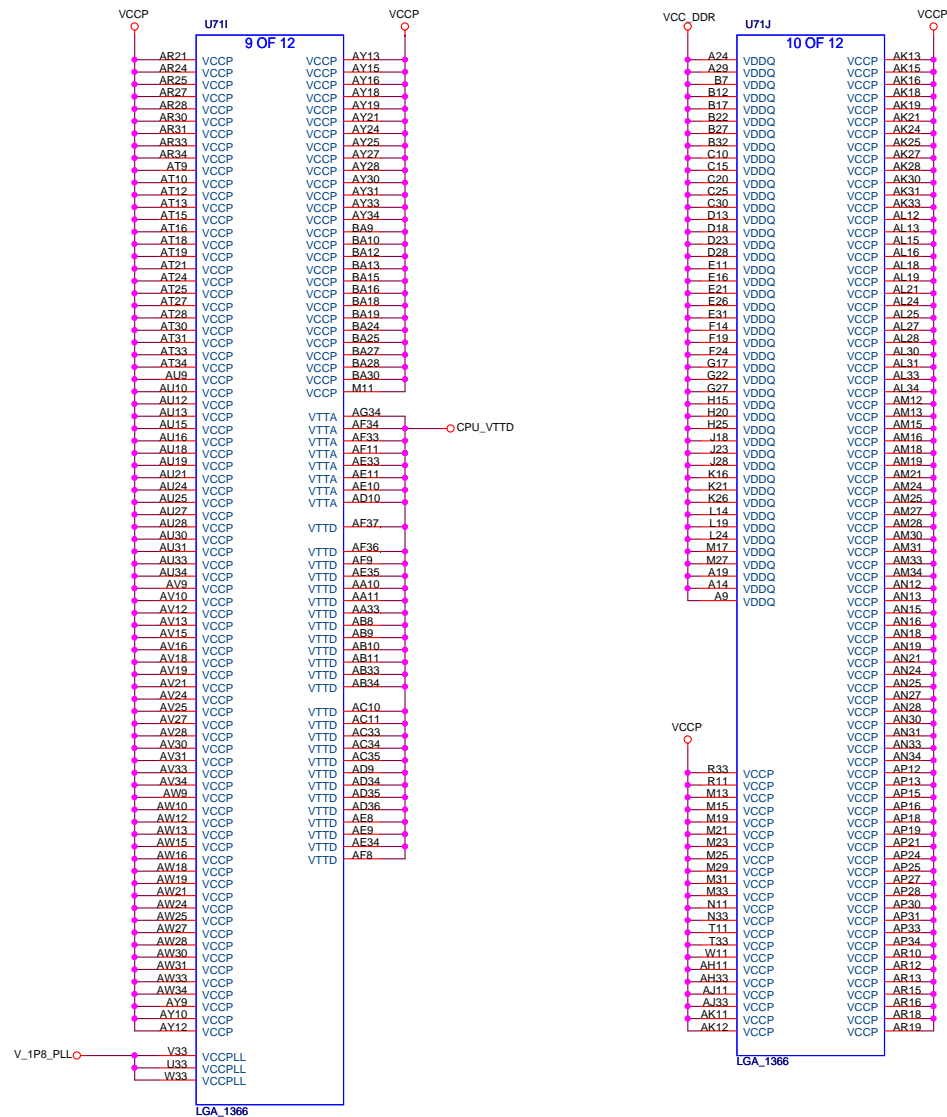
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DATA B3	Y34	DDR1_DQ_3	DDR1_DQS_P1	R37	QDS_B#1	10			
DATA B4	AA35	DDR1_DQ_4	DDR1_DQS_N1						
DATA B5	AB36	DDR1_DQ_5		L35	QDS_B2	10			
DATA B6	Y35	DDR1_DQ_6	DDR1_DQS_P2	L36	QDS_B#2	10			
DATA B7	Y40	DDR1_DQ_7	DDR1_DQS_N2						
DATA B8	P34	DDR1_DQ_8		L30	QDS_B3	10			
DATA B9	P35	DDR1_DQ_9	DDR1_DQS_P3	L31	QDS_B#3	10			
DATA B10	P38	DDR1_DQ_10	DDR1_DQS_N3						
DATA B11	N39	DDR1_DQ_11		E7	QDS_B4	10			
DATA B12	R34	DDR1_DQ_12	DDR1_DQS_P4	D7	QDS_B#4	10			
DATA B13	R35	DDR1_DQ_13	DDR1_DQS_N4						
DATA B14	N37	DDR1_DQ_14		H6	QDS_B5	10			
DATA B15	N38	DDR1_DQ_15	DDR1_DQS_P5	G6	QDS_B#5	10			
DATA B16	M35	DDR1_DQ_16	DDR1_DQS_N5						
DATA B17	M34	DDR1_DQ_17		L6	QDS_B6	10			
DATA B18	K35	DDR1_DQ_18	DDR1_DQS_P6	L5	QDS_B#6	10			
DATA B19	J35	DDR1_DQ_19	DDR1_DQS_N6						
DATA B20	N34	DDR1_DQ_20		Y8	QDS_B7	10			
DATA B21	M36	DDR1_DQ_21	DDR1_DQS_P7	Y9	QDS_B#7	10			
DATA B22	J36	DDR1_DQ_22	DDR1_DQS_N7						
DATA B23	H36	DDR1_DQ_23		G33					
DATA B24	H33	DDR1_DQ_24	DDR1_DQS_P8	G34					
DATA B25	L33	DDR1_DQ_25	DDR1_DQS_N8						
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DATA B27	J32	DDR1_DQ_27	DDR1_DQS_P9	AA45					
DATA B28	H34	DDR1_DQ_28	DDR1_DQS_N9						
DATA B29	H34	DDR1_DQ_29		P36					
DATA B30	L32	DDR1_DQ_30	DDR1_DQS_P10	P37					
DATA B31	K30	DDR1_DQ_31	DDR1_DQS_N10						
DATA B32	E8	DDR1_DQ_32		L37					
DATA B33	E8	DDR1_DQ_33	DDR1_DQS_P11	K37					
DATA B34	E5	DDR1_DQ_34	DDR1_DQS_N11						
DATA B35	F5	DDR1_DQ_35		K34					
DATA B36	F10	DDR1_DQ_36	DDR1_DQS_P12	K33					
DATA B37	G8	DDR1_DQ_37	DDR1_DQS_N12						
DATA B38	D6	DDR1_DQ_38		F8					
DATA B39	F6	DDR1_DQ_39	DDR1_DQS_P13	F7					
DATA B40	H6	DDR1_DQ_40	DDR1_DQS_N13						
DATA B41	J6	DDR1_DQ_41		H7					
DATA B42	G4	DDR1_DQ_42	DDR1_DQS_P14	J7					
DATA B43	H4	DDR1_DQ_43	DDR1_DQS_N14						
DATA B44	G8	DDR1_DQ_44		M5					
DATA B45	H8	DDR1_DQ_45	DDR1_DQS_P15	M4					
DATA B46	G5	DDR1_DQ_46	DDR1_DQS_N15						
DATA B47	J5	DDR1_DQ_47		Y4					
DATA B48	K4	DDR1_DQ_48	DDR1_DQS_P16	Y5					
DATA B49	K5	DDR1_DQ_49	DDR1_DQS_N16						
DATA B50	R5	DDR1_DQ_50		F35					
DATA B51	T5	DDR1_DQ_51	DDR1_DQS_P17	F35					
DATA B52	J4	DDR1_DQ_52	DDR1_DQS_N17						
DATA B53	M6	DDR1_DQ_53							
DATA B54	R8	DDR1_DQ_54							
DATA B55	R7	DDR1_DQ_55							
DATA B56	W6	DDR1_DQ_56							
DATA B57	W7	DDR1_DQ_57							
DATA B58	Y10	DDR1_DQ_58							
DATA B59	W10	DDR1_DQ_59							
DATA B60	V9	DDR1_DQ_60							
DATA B61	W5	DDR1_DQ_61							
DATA B62	AA7	DDR1_DQ_62							
DATA B63	W9	DDR1_DQ_63							
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E36		DDR1_ECC_1							
E33		DDR1_ECC_2							
G36		DDR1_ECC_3							
E37		DDR1_ECC_4							
E34		DDR1_ECC_5							
G35		DDR1_ECC_6							
		DDR1_ECC_7							

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U71C 3 OF 12									
DATA C0	W34	DDR2_DQ_0	DDR2_DQS_P0	W37	QDS_C0	11			
DATA C1	W35	DDR2_DQ_1	DDR2_DQS_N0	W36	QDS_C#0	11			
DATA C2	V36	DDR2_DQ_2							
DATA C3	U36	DDR2_DQ_3	DDR2_DQS_P1	T37	QDS_C1	11			
DATA C4	U34	DDR2_DQ_4	DDR2_DQS_N1	T38	QDS_C#1	11			
DATA C5	V34	DDR2_DQ_5							
DATA C6	V37	DDR2_DQ_6	DDR2_DQS_P2	K40	QDS_C2	11			
DATA C7	V39	DDR2_DQ_7	DDR2_DQS_N2	K39	QDS_C#2	11			
DATA C8	U38	DDR2_DQ_8							
DATA C9	U39	DDR2_DQ_9	DDR2_DQS_P3	E39	QDS_C3	11			
DATA C10	R39	DDR2_DQ_10	DDR2_DQS_N3	E40	QDS_C#3	11			
DATA C11	T36	DDR2_DQ_11							
DATA C12	W39	DDR2_DQ_12	DDR2_DQS_P4	J10	QDS_C4	11			
DATA C13	V39	DDR2_DQ_13	DDR2_DQS_N4	J9	QDS_C#4	11			
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DATA C15	R40	DDR2_DQ_15	DDR2_DQS_P5	K7	QDS_C#5	11			
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DATA C18	J40	DDR2_DQ_18	DDR2_DQS_P6	P5	QDS_C#6	11			
DATA C19	J39	DDR2_DQ_19	DDR2_DQS_N6						
DATA C20	P40	DDR2_DQ_20		U8	QDS_C7	11			
DATA C21	N36	DDR2_DQ_21	DDR2_DQS_P7	T8	QDS_C#7	11			
DATA C22	L40	DDR2_DQ_22	DDR2_DQS_N7						
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DATA C24	G40	DDR2_DQ_24	DDR2_DQS_P8	G30					
DATA C25	F40	DDR2_DQ_25	DDR2_DQS_N8						
DATA C26	J37	DDR2_DQ_26		U35					
DATA C27	H37	DDR2_DQ_27	DDR2_DQS_P9	T35					
DATA C28	H39	DDR2_DQ_28	DDR2_DQS_N9						
DATA C29	G39	DDR2_DQ_29		U40					
DATA C30	F38	DDR2_DQ_30	DDR2_DQS_P10	T40					
DATA C31	E38	DDR2_DQ_31	DDR2_DQS_N10						
DATA C32	K12	DDR2_DQ_32		M38					







U71K		
11 OF 12		
B42	VSS	AV23
B37	VSS	AV22
B2	VSS	AV20
A41	VSS	AV17
A39	VSS	AV14
A35	VSS	AV11
A6	VSS	AV4
A4	VSS	AU43
C6	VSS	AU36
F6	VSS	AU35
E1	VSS	AU32
D43	VSS	AU29
D38	VSS	AU26
D33	VSS	AU23
D8	VSS	AU22
D3	VSS	AU20
C43	VSS	AU17
C40	VSS	AU14
C35	VSS	AU11
E36	VSS	AU5
F41	VSS	AU1
F4	VSS	AT41
F9	VSS	AT38
F29	VSS	AT35
F34	VSS	AT32
F39	VSS	AT29
G2	VSS	AT26
G7	VSS	AT23
G12	VSS	AT22
G32	VSS	AT20
G37	VSS	AT17
G42	VSS	AT14
H5	VSS	AT11
H10	VSS	AT8
H30	VSS	AT7
H35	VSS	AR39
BA39	VSS	AR35
BA35	VSS	AR32
BA29	VSS	AR29
BA26	VSS	AR26
BA20	VSS	AR23
BA17	VSS	AR22
BA14	VSS	AR20
BA11	VSS	AR17
BA5	VSS	AR14
BA3	VSS	AR11
AY42	VSS	AR3
AY37	VSS	AP36
AY32	VSS	AP35
AY29	VSS	AP32
AY26	VSS	AP29
AY23	VSS	AP26
AY22	VSS	AP23
AY20	VSS	AP22
AY17	VSS	AP20
AY14	VSS	AP17
AY11	VSS	AP14
AY7	VSS	AP11
AW35	VSS	AP10
AW32	VSS	AP6
AW29	VSS	AP5
AW26	VSS	AP1
AW23	VSS	AN20
AW22	VSS	AN17
AW20	VSS	AN14
AW17	VSS	AN11
AW14	VSS	
AW11	VSS	
AW8	VSS	
AW6	VSS	
AW1	VSS	
AV41	VSS	
AV39	VSS	
AV32	VSS	
AV29	VSS	
AV26	VSS	

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U71L		
12 OF 12		
AN7	VSS	AB40
AN3	VSS	AB37
AM39	VSS	AB7
AM37	VSS	AB4
AM35	VSS	AA39
AM32	VSS	AA38
AM29	VSS	AA34
AM26	VSS	AA9
AM23	VSS	AA3
AM22	VSS	Y41
AM20	VSS	Y36
AM17	VSS	Y33
AM14	VSS	Y11
AM11	VSS	Y6
AM9	VSS	Y1
AM5	VSS	W43
AL42	VSS	W38
AL37	VSS	W8
AL36	VSS	W3
AL35	VSS	V40
AL32	VSS	V35
AL29	VSS	V10
AL26	VSS	V5
AL23	VSS	U42
AL22	VSS	U37
AL20	VSS	U7
AL17	VSS	U2
AL14	VSS	T39
AL11	VSS	T34
AL7	VSS	T9
AL2	VSS	T4
AL1	VSS	R41
AK3	VSS	R36
AK39	VSS	R6
AK34	VSS	R1
AK32	VSS	P43
AK29	VSS	P38
AK26	VSS	P33
AK23	VSS	P11
AK22	VSS	P8
AK20	VSS	P3
AK17	VSS	N40
AK14	VSS	N35
AK10	VSS	N10
AK9	VSS	N6
AK3	VSS	M42
AJ41	VSS	M37
AJ36	VSS	M32
AJ34	VSS	M30
AJ5	VSS	M28
AH39	VSS	M26
AH37	VSS	M24
AH34	VSS	M22
AH7	VSS	M20
AH1	VSS	M18
AG43	VSS	M16
AG33	VSS	M14
AG11	VSS	M12
AG9	VSS	M7
AG3	VSS	M2
AF41	VSS	L39
AF38	VSS	L34
AF35	VSS	L29
AF5	VSS	L9
AE39	VSS	L4
AE7	VSS	K41
AE2	VSS	K36
AD43	VSS	K31
AD41	VSS	K11
AD33	VSS	K6
AD11	VSS	K1
AD37	VSS	J43
AC36	VSS	J38
AC9	VSS	J33
AC5	VSS	J13
AC2	VSS	J8
AB42	VSS	J3
AC7	VSS	H40

LGA_1366

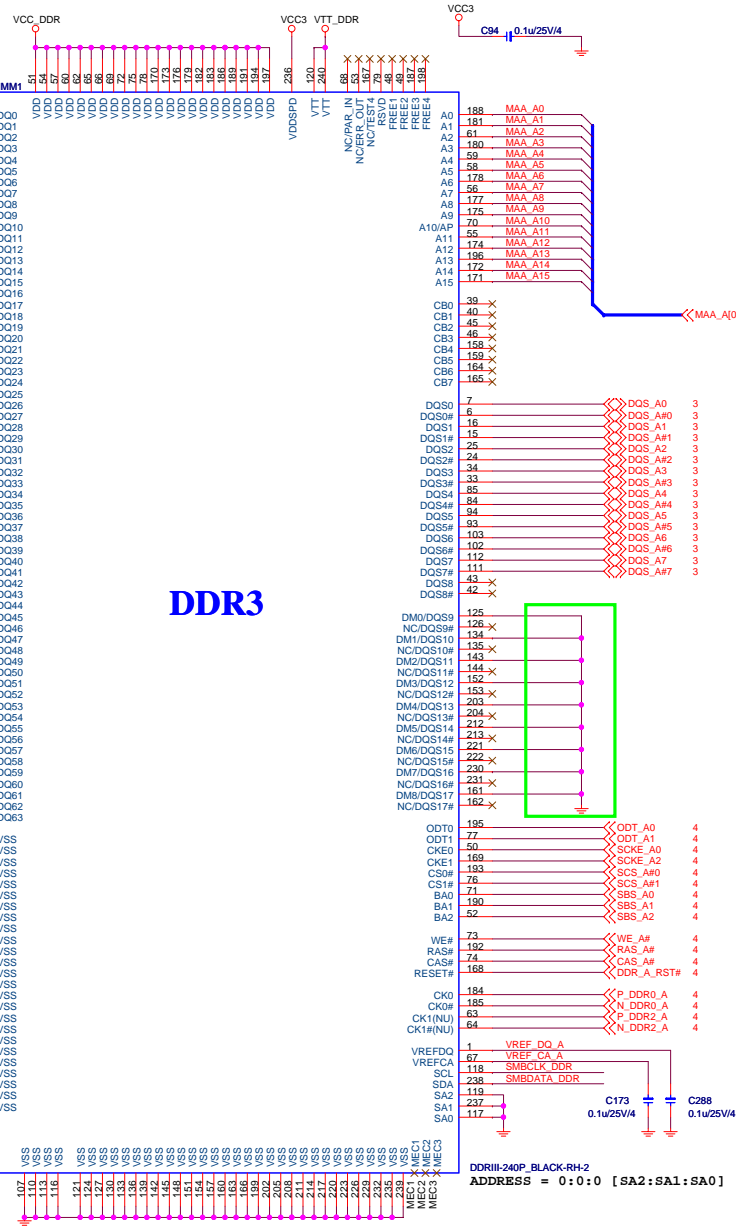
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8 OF 12		
AM8	RSVD	AC8
AL8	RSVD	AD8
AM6	RSVD	AD5
AM7	RSVD	AD6
AN6	RSVD	AD7
AM4	RSVD	AD8
AN4	RSVD	AC6
AP4	RSVD	AC4
AP4	RSVD	AD4
AM2	RSVD	AE3
AM3	RSVD	AE4
AN1	RSVD	AC3
AM1	RSVD	AB3
AP2	RSVD	AD2
AN2	RSVD	AD3
AR4	RSVD	AE1
AR6	RSVD	AD1
AT1	RSVD	AE2
AR1	RSVD	AF3
AT3	RSVD	AH2
AT2	RSVD	AC2
AL4	RSVD	AH3
AU3	RSVD	AH4
AW4	RSVD	AK1
AW3	RSVD	AJ1
AU7	RSVD	AJ3
AU6	RSVD	AJ2
AY6	RSVD	AG7
AY5	RSVD	AG6
BA7	RSVD	AJ4
BA6	RSVD	AK4
AV5	RSVD	AK6
AW5	RSVD	AK5
AY8	RSVD	AH6
BA8	RSVD	AJ6
AV7	RSVD	AJ8
AW7	RSVD	AJ7
AU8	RSVD	AG8
AV8	RSVD	AH8
AT6	RSVD	
AR6	RSVD	
AE6	RSVD	
AE6	RSVD	AL6

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DIMM1 / CHANNEL A0

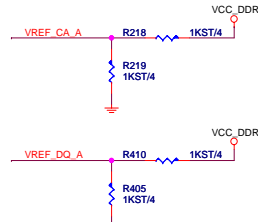
Place DIMM Socket Power Plane

Close to the DIMM VTT_DDR Pin

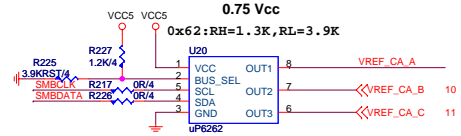


DDR3

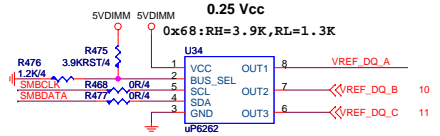
UPI VOLTAGE CONSOLE



0.75 Vcc
0x62:RH=1.3K,RL=3.9K



0.25 Vcc
0x68:RH=3.9K,RL=1.3K



10,11 SMBCLK_DDR >> R192 33/4 >> SMBCLK
10,11 SMBDATA_DDR >> R191 33/4 >> SMBDATA

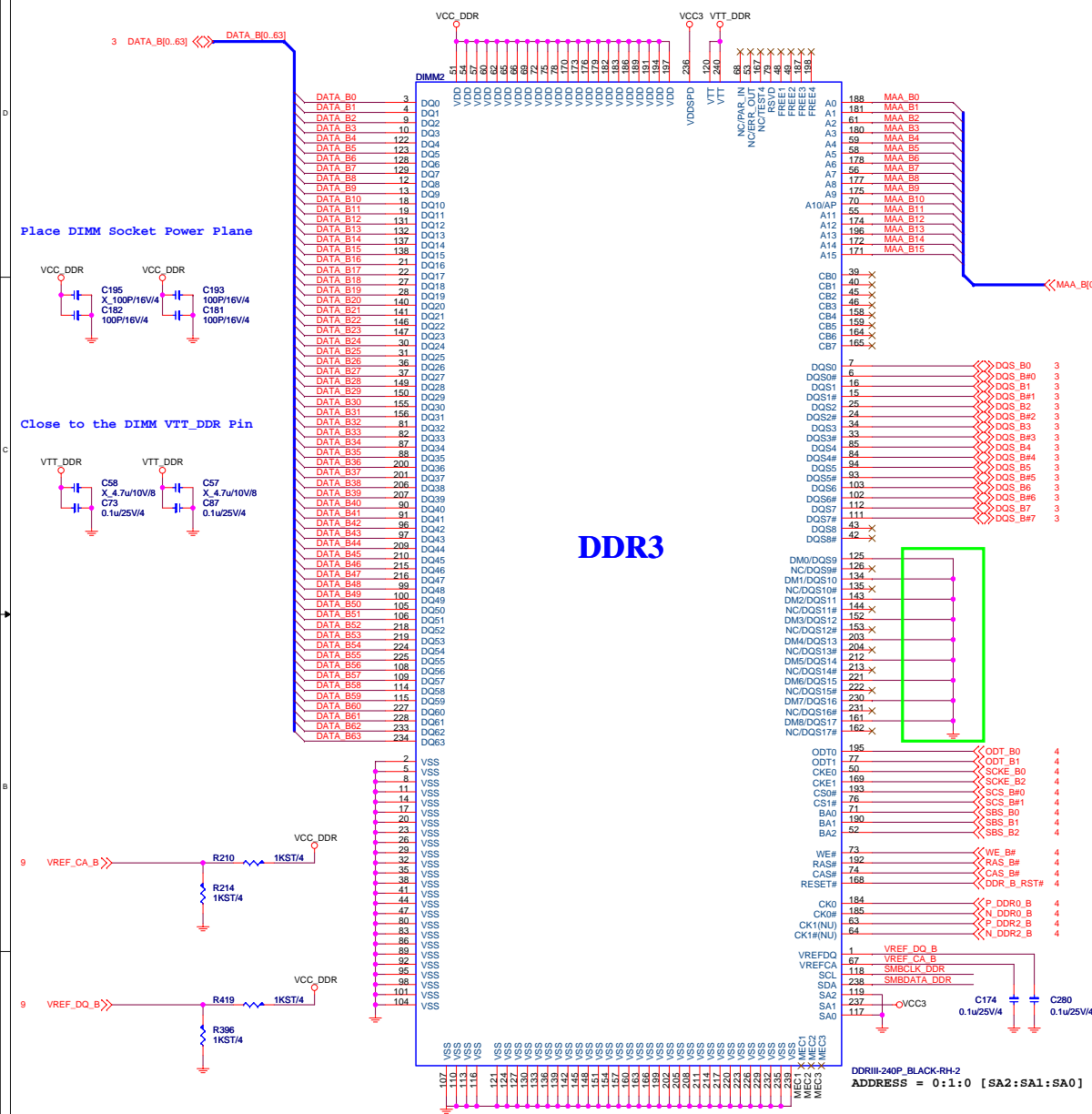
MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

DDR III DIMM1

Size	Document Number	Rev
Custom	DELL Suzuki MLK (MS-7543)	0B

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DIMM2 / CHANNEL B0



Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR_IN. When in single ended mode used for DQS0-DQS7.

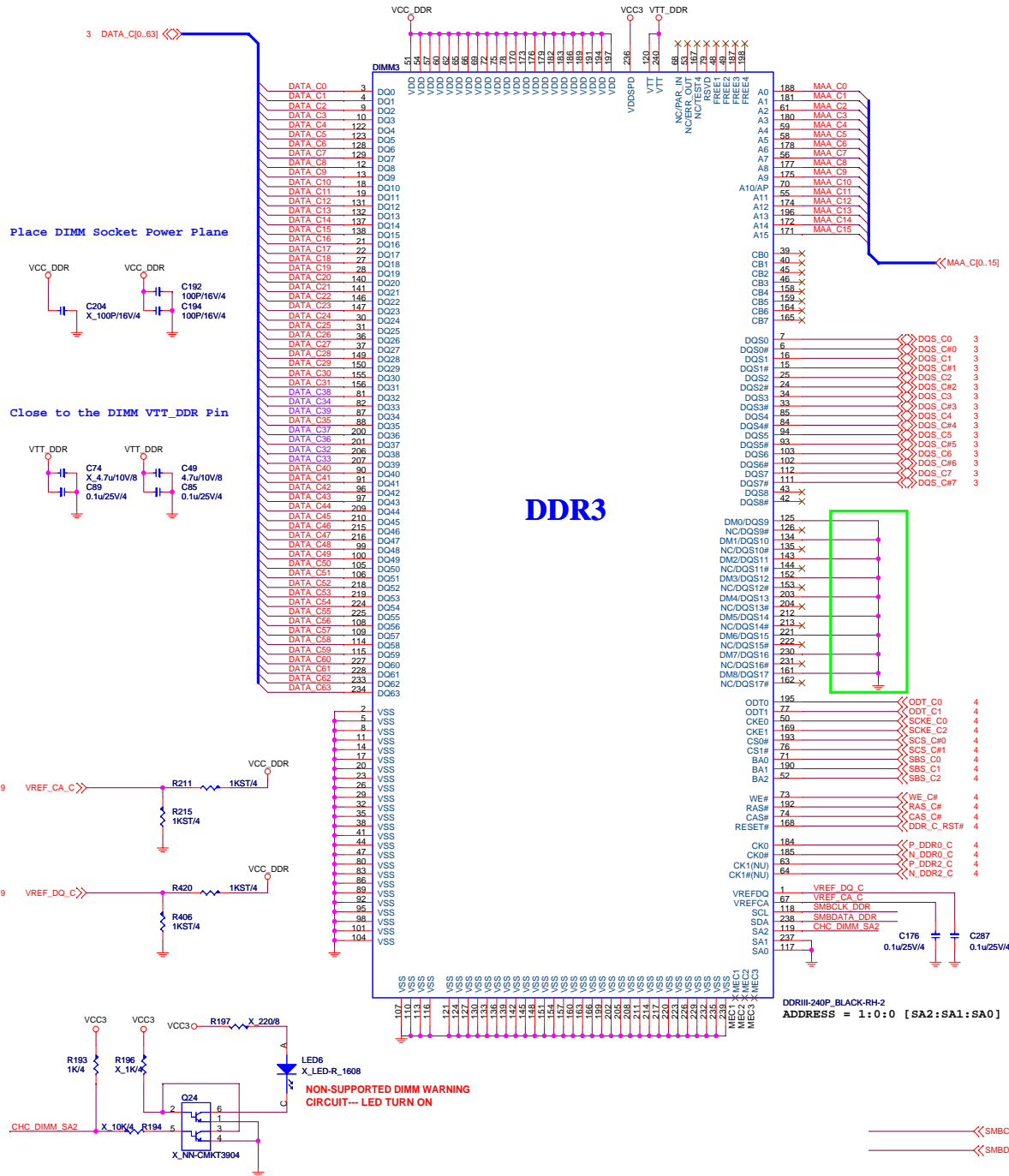
Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

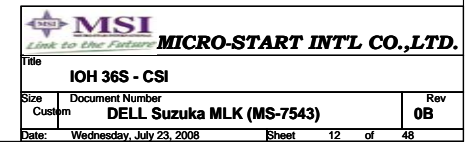
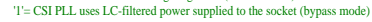
RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

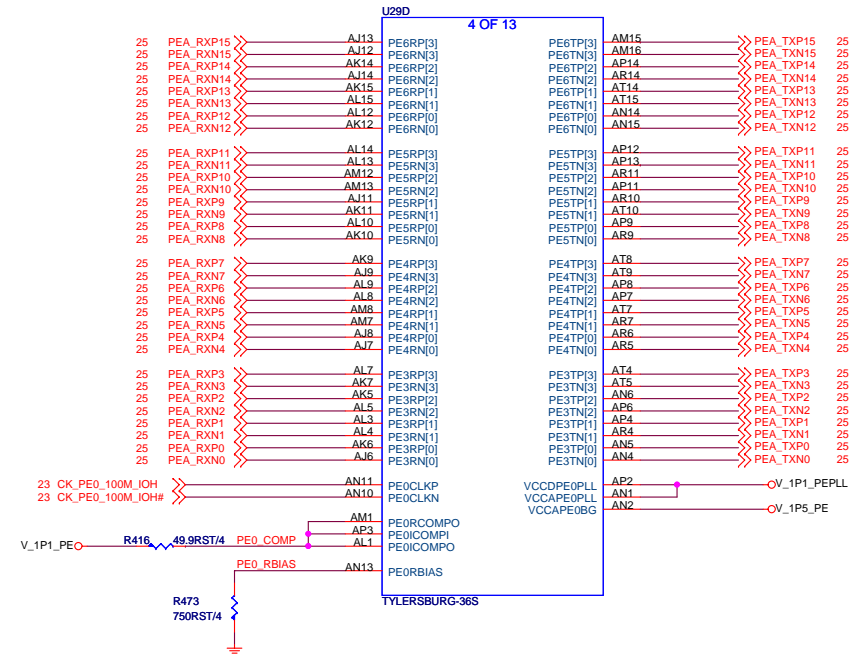
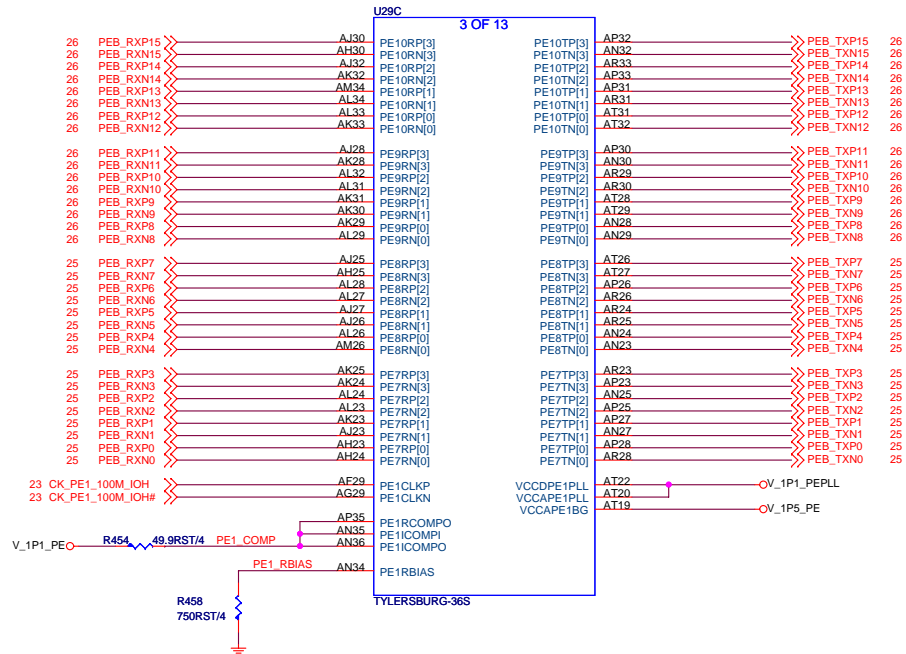
◀ SMCCLK_DDR 9,11
◀ SMCBDATA_DDR 9,11

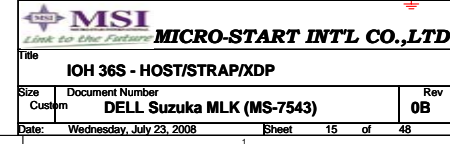
MICRO-START INT'L CO.,LTD.	
Title	
DDR III DIMM2	
Size	Document Number
Custom	DELL Suzuka MLK (MS-7543)
Date:	Wednesday, July 23, 2008
Sheet	10 of 48
Rev	0B

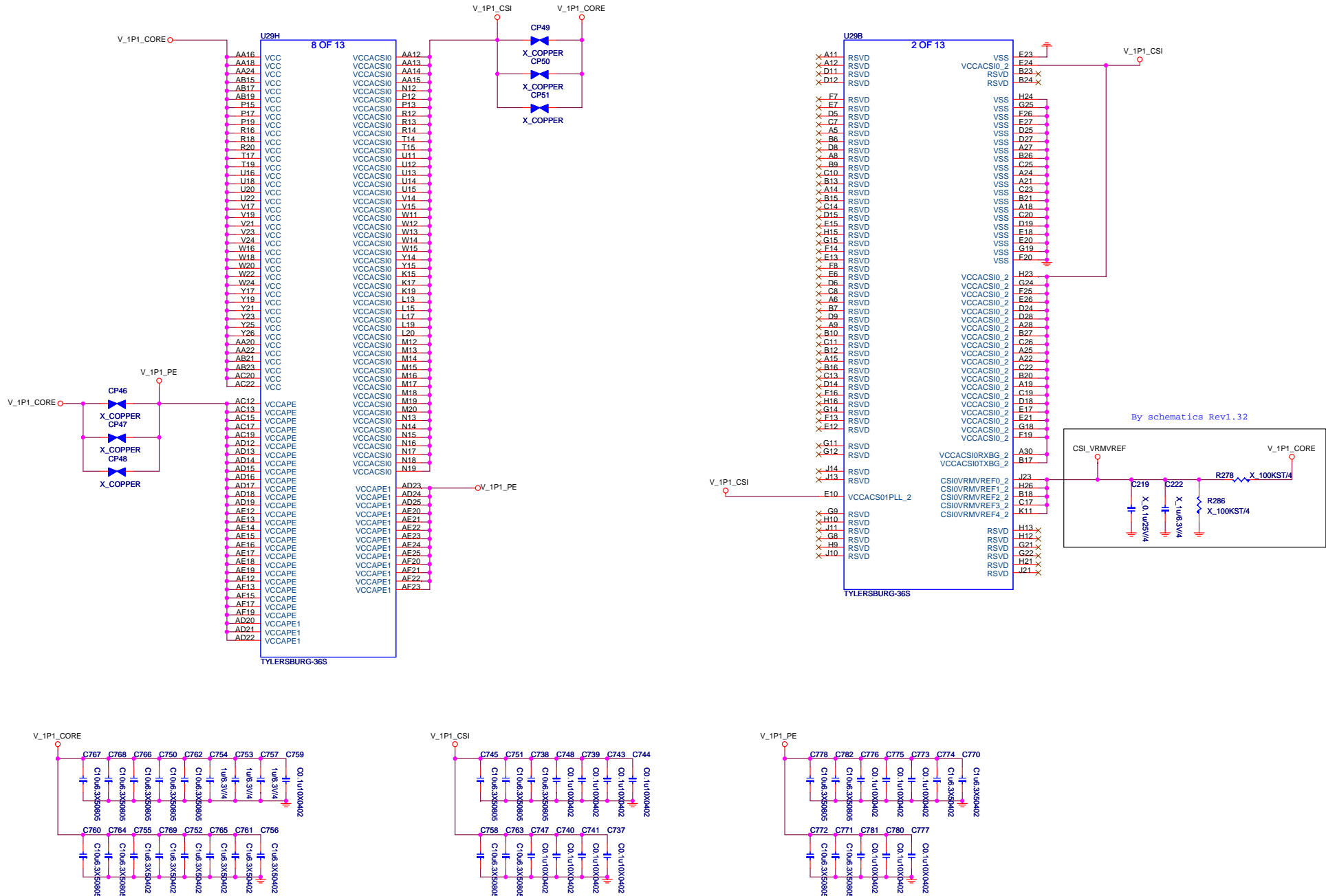
DIMM3 / CHANNEL C0

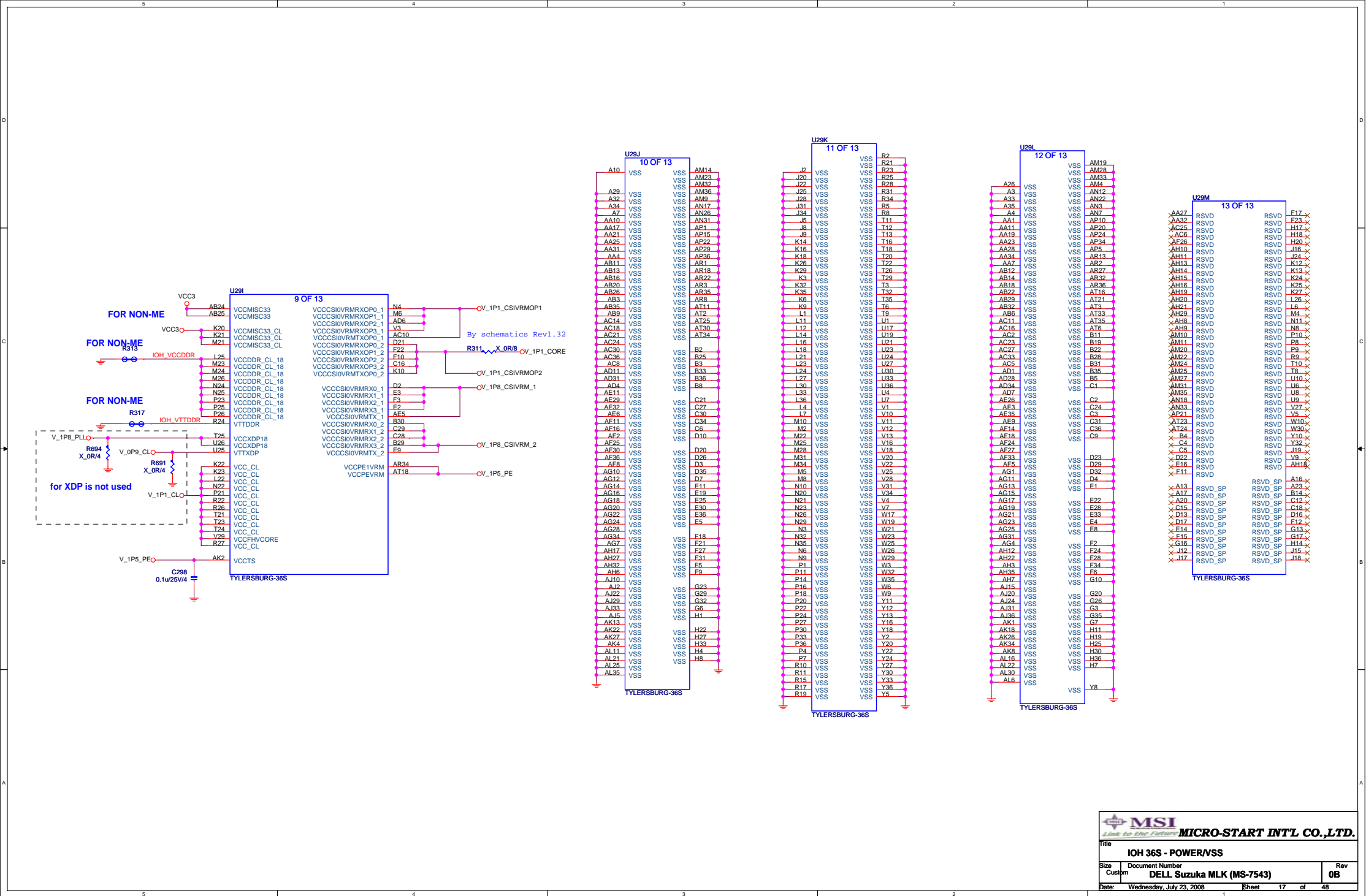










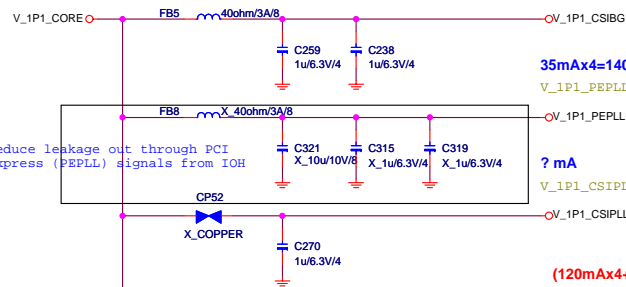


V_1P1_CORE REPLACE WITH V_1P1_VCCA

0.7A???

10mA \times 2=20mA

V_1P1_CSIBG = CSIBG_RX+CSIBG_TX



35mA \times 4=140mA

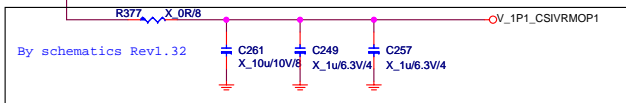
V_1P1_PEPLL = PEPLLA+PEPLLD

? mA

V_1P1_CSIPLL = CSI_PLL

(120mA \times 4+60mA)??=0.54A ?????

V_1P1_CSIVRMOP1 = CSIVRMOP_RX[1:4]+CSIVRMOP_TX1



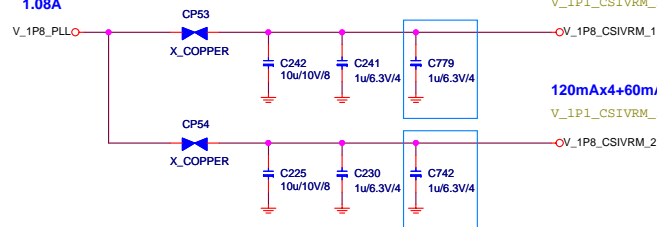
1.08A

120mA \times 4+60mA=0.54A

V_1P1_CSIVRM_1 = CSIVRM_RX_1+CSIVRM1_TX_1

120mA \times 4+60mA=0.54A

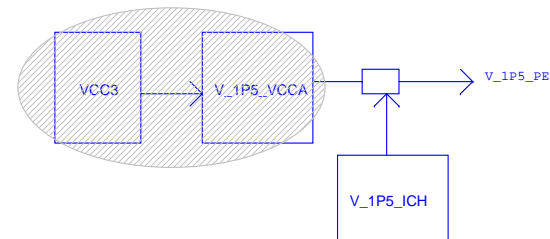
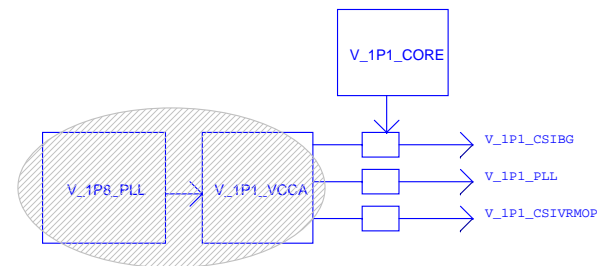
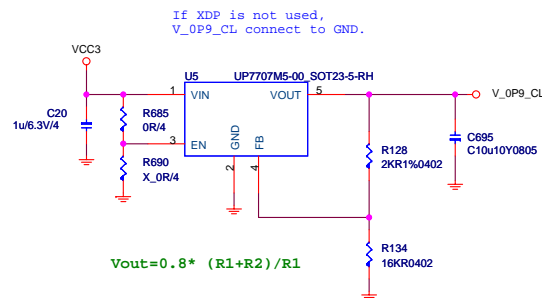
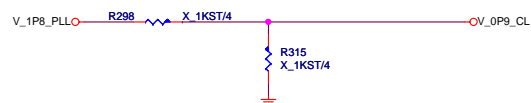
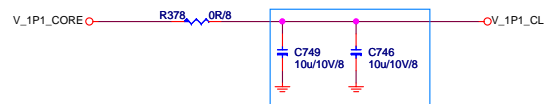
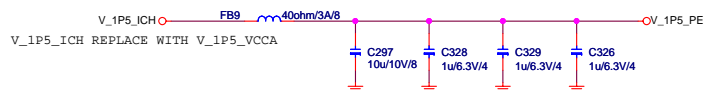
V_1P1_CSIVRM_2 = CSIVRM_RX_2+CSIVRM1_TX_2



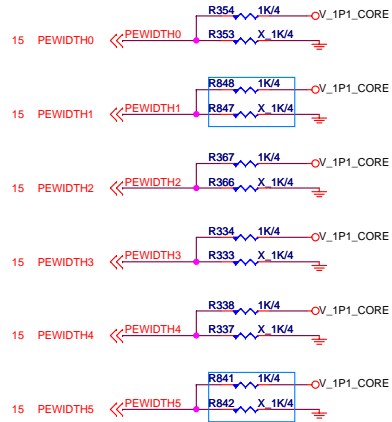
186.3mA+?

92mA \times 2+1.15mA \times 2+=186.3mA+?

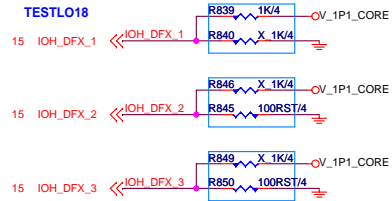
V_1P5_PE = PEVRM+PEBG0+PEBG1+VCCTS



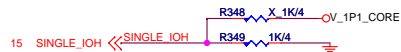
PEWIDTH0-5
PCIE Link Width Select
"111011" = 2x16
"101111" = 4x8
"011111" = Wait On Bios



IOH_DFX_2, 3}
DDR frequency selection pins:
DDRFRFREQ[3:2] as DDR frequency selection defined as:
"00" = 133MHz input, 200MHz core
"01" = 100 MHz input, 200MHz core
"10" = RSVD
"11" = RSVD



SINGLE_IOH
Used for dual TBG IOH selection:
"0": IOH is not connected to another IOH on some CSI link (default)
"1": IOH is connected to another IOH on some CSI link



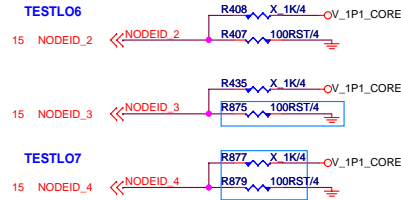
CL_CLK_SRC
Used for ME default clock source:
"1": PLL (default) -- EXT ME CLK
"0": Ring Oscillator (back-up) -- INT ME CLK



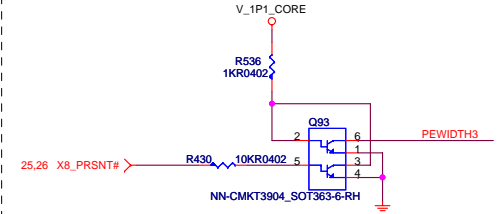
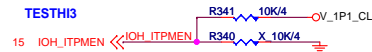
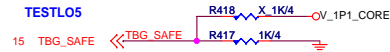
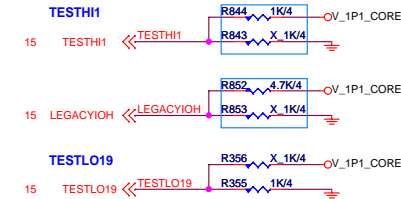
NON-ME FUNCTION

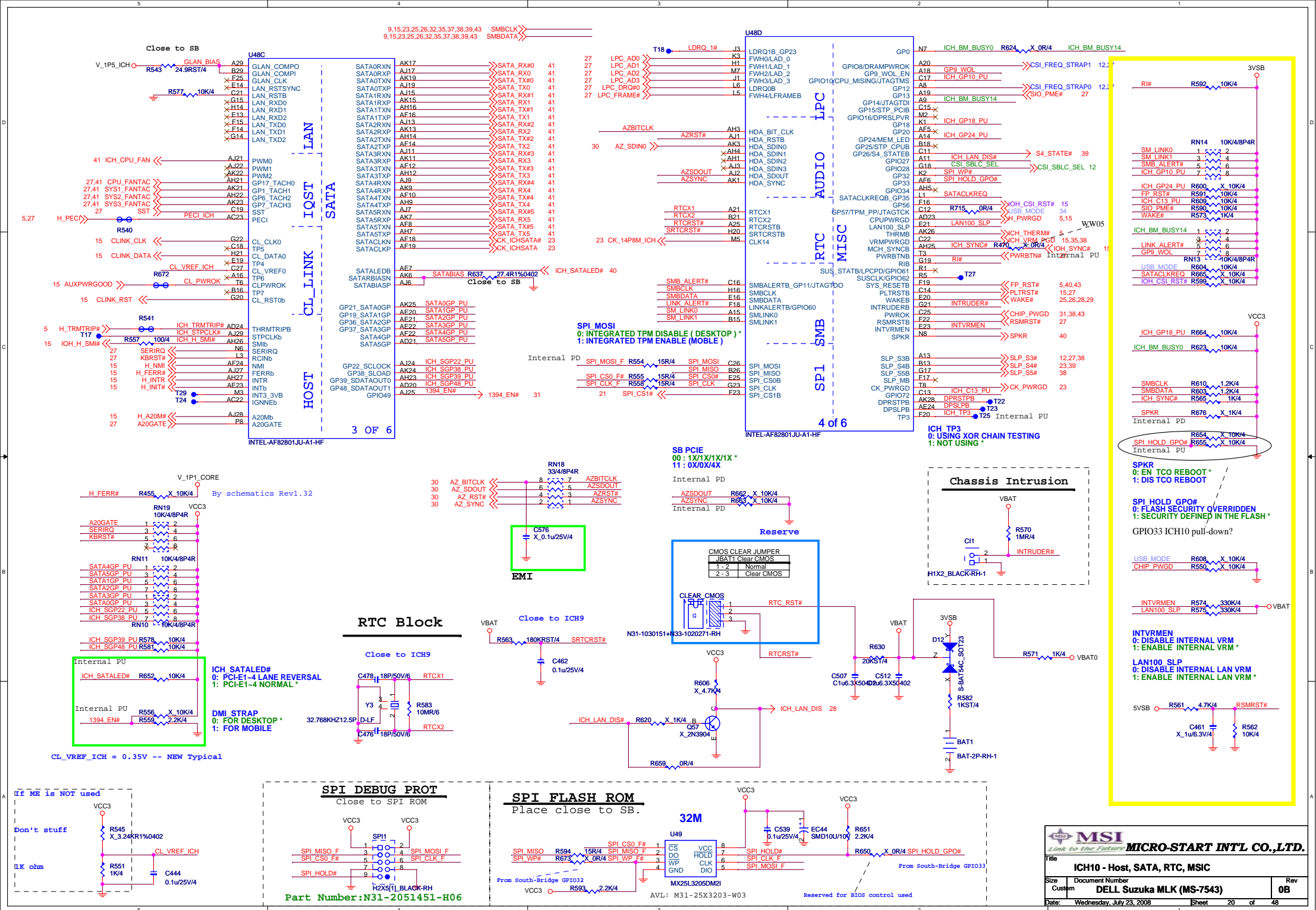
VCCADDRPLL and ME_CLK_SRC
pins must be tied to VSS as well

NODEID_3_TBG
For dual TBG IOH configuration,
it indicates which CSI port is connected to the other IOH.
"0": CSI0
"1": CSI1

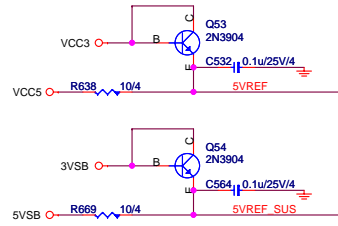


LEGACYIOH
Used to determine legacy or non-legacy selection:
"1": Legacy IOH
"0": Non-legacy IOH

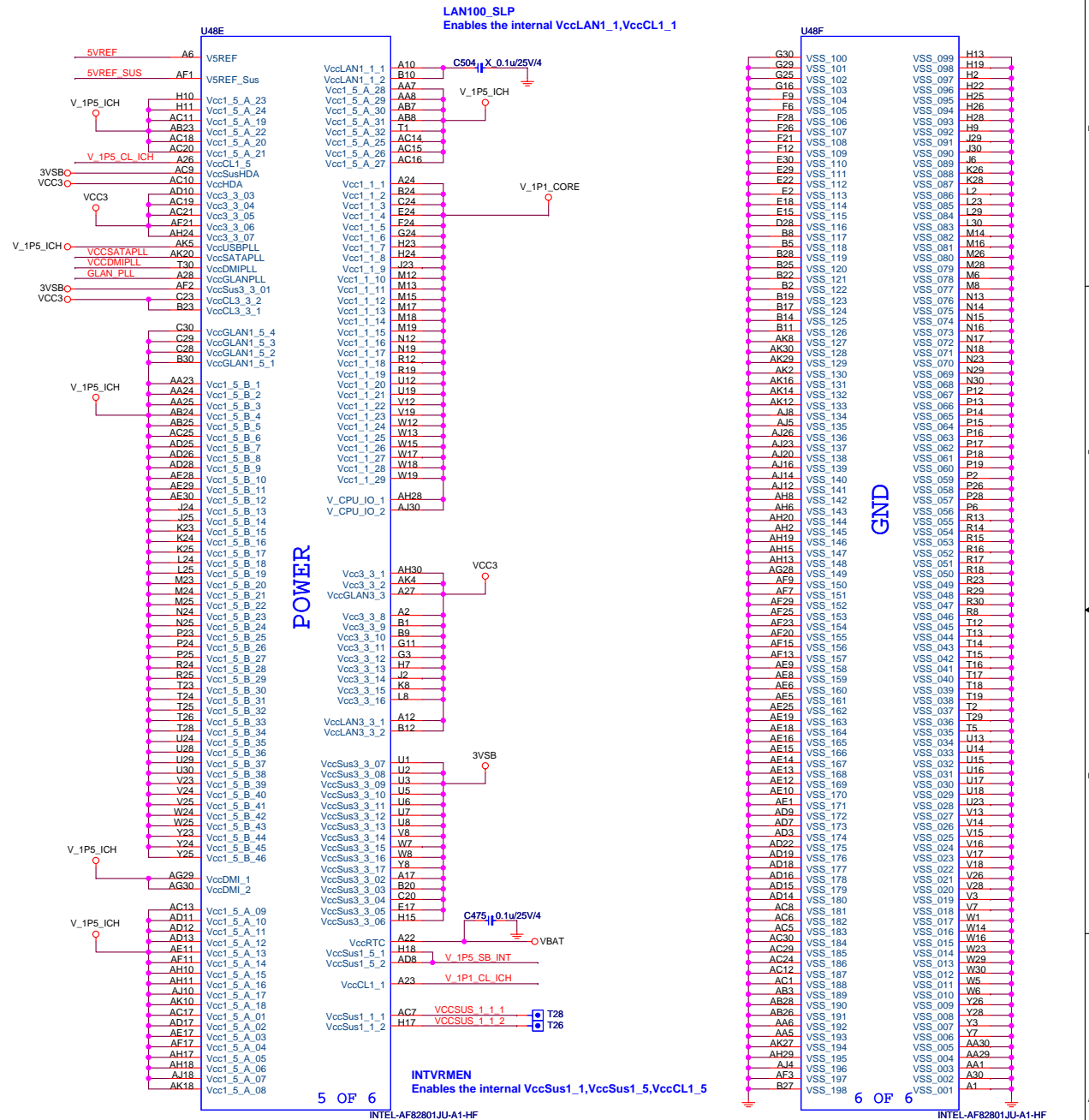
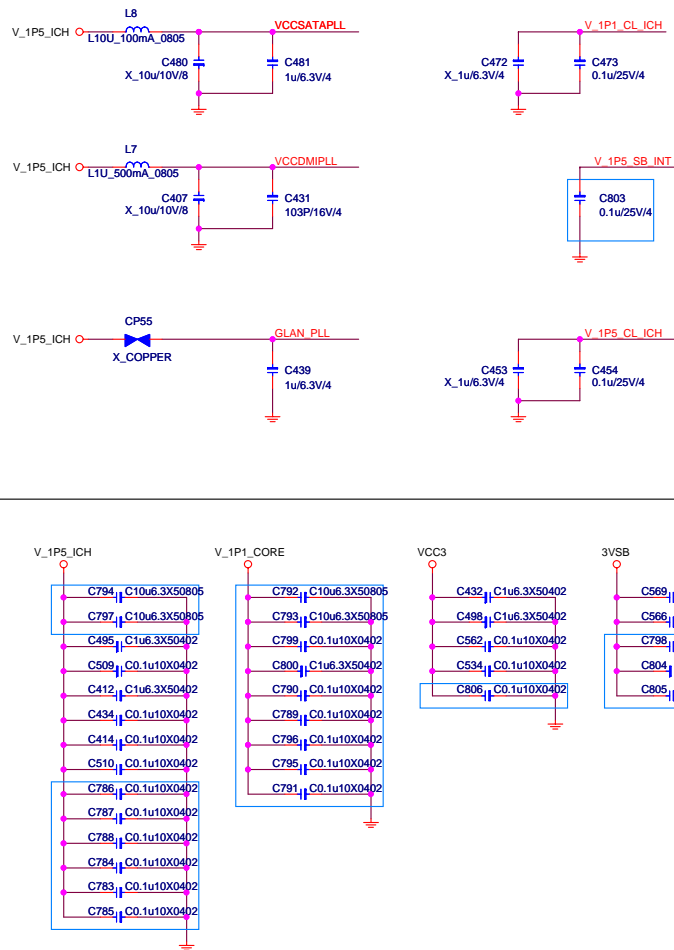




5VREF & 5VREF_SUS Sequencing Circuit



SB POWER



[illegible]

0: Pin21/22 100MHz*
1: Pin21/22 96MHz

GSEL_33M_CLK **R643** **X 4.7K/4**

Internal pull down

0: PCICLK4
1: RESET*

_WDT#_R **R642** **4.7K/4**

Internal pull down

0: PCIE9*
1: CPU_I2P

I2P_EN **R605** **X 4.7K/4**

Internal pull down

1: 25MHz freerun function

CK_25M_0F **R641** **X 4.7K/4**

R646 **X 4.7K/4**

Internal pull up

1 = Selects pin 29/30 to be PCI_STOP#/CPU_STOP#

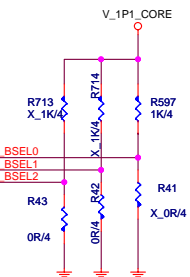
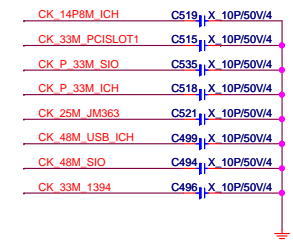
CK_25M_1 **R647** **X 4.7K/4**

Internal pull down

For ICS CPU/DIV SEL
0: FSLD BIT3 = 0*
1: FSLD BIT3 = 1

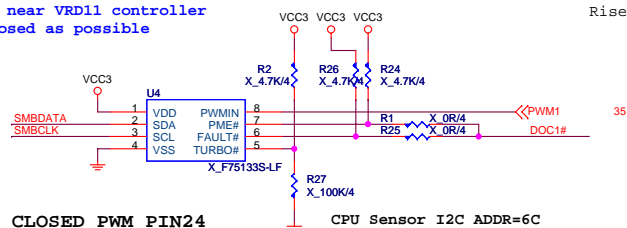
FSD_33M_CLK **R631** **4.7K/4**

Internal pull up



BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHz
0	0	1	133 MHz (default)
0	1	0	200 MHz
0	1	1	166 MHz
1	0	0	333 MHz
1	0	1	100 MHz
1	1	0	400 MHz
1	1	1	200 MHz

Place near VRD11 controller
as closed as possible



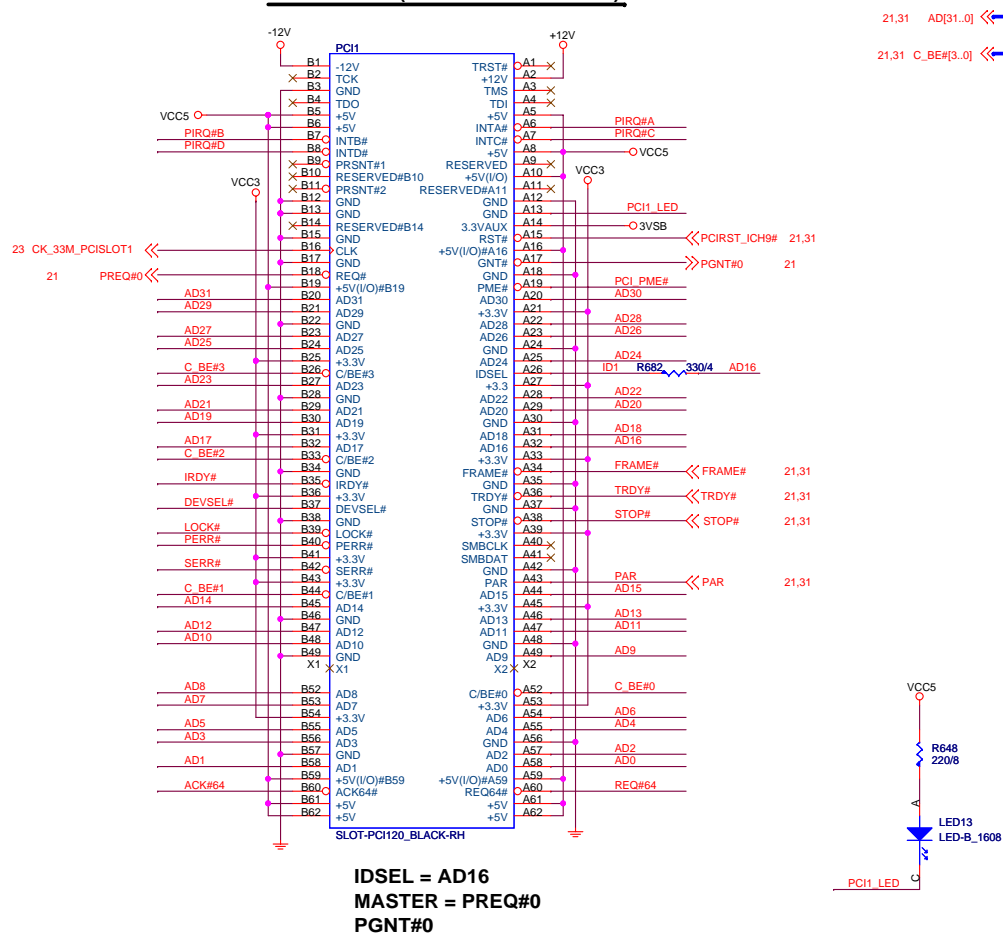
```
Vimon= (Riout / N) x (Rx/Risen) x Iload
Riout = Rimon
Rx = DCR
Risen = ISEN+
```

DOC#0	DOC#1	Over-clk
1	1	15%
0	1	10%
1	0	5%
0	0	Normal

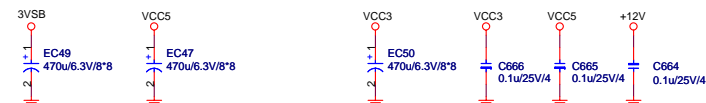
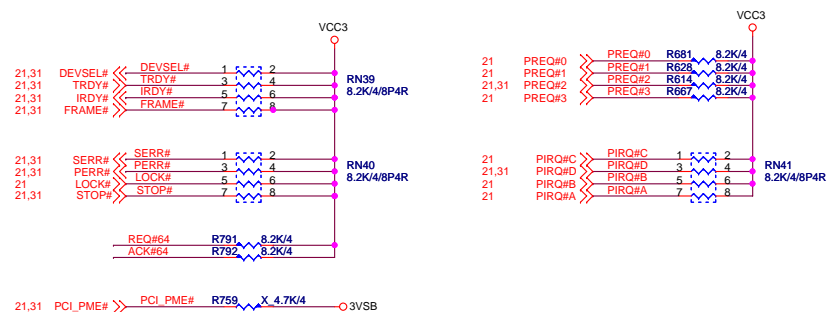
 **MSI**
Link to the Future **MICRO-START INT'L CO., LTD.**

Title			
Clock Gen ICS9LPRS113			
Size	Document Number	Rev	
Custom	DELL Suzuka MLK (MS-7543)	0B	
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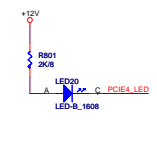
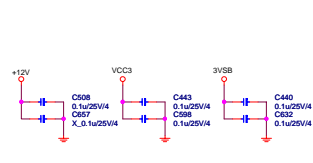
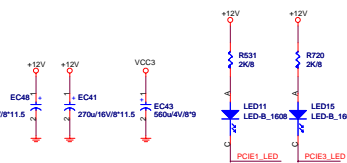
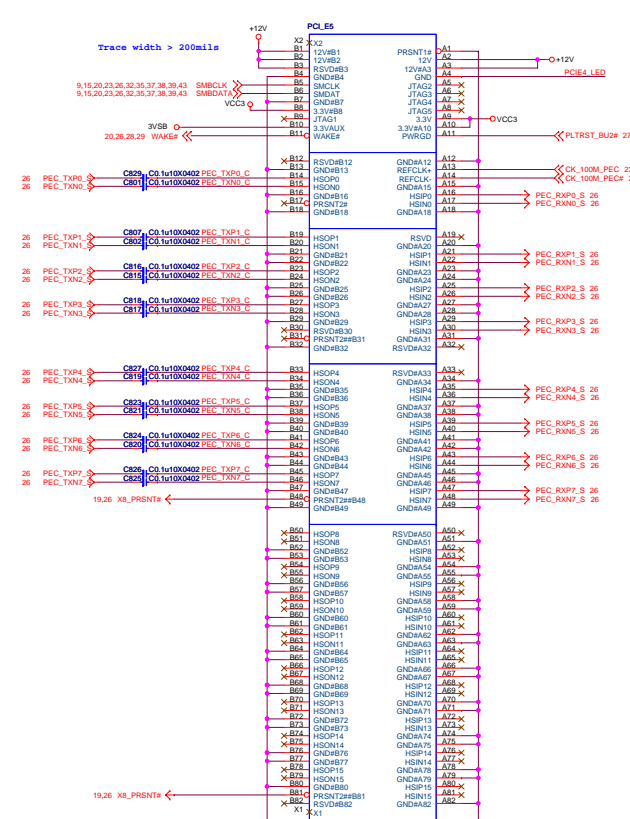
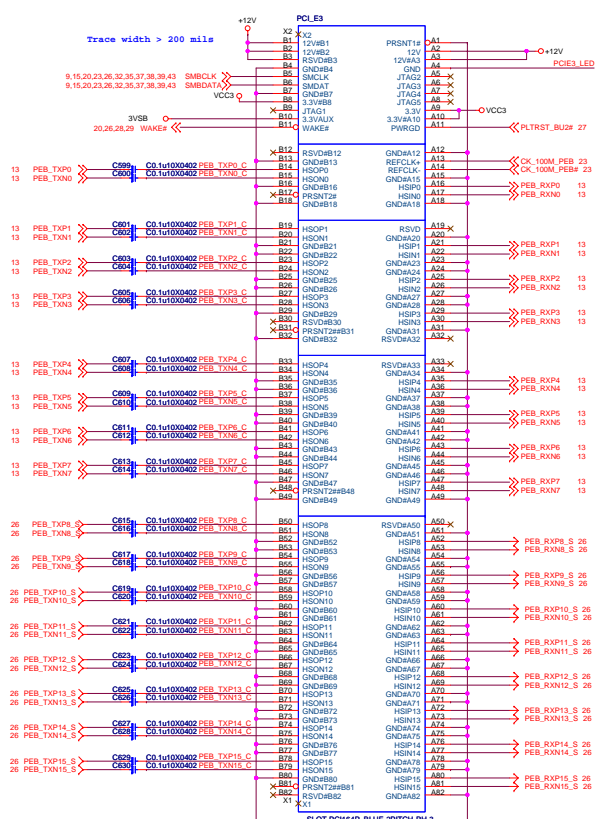
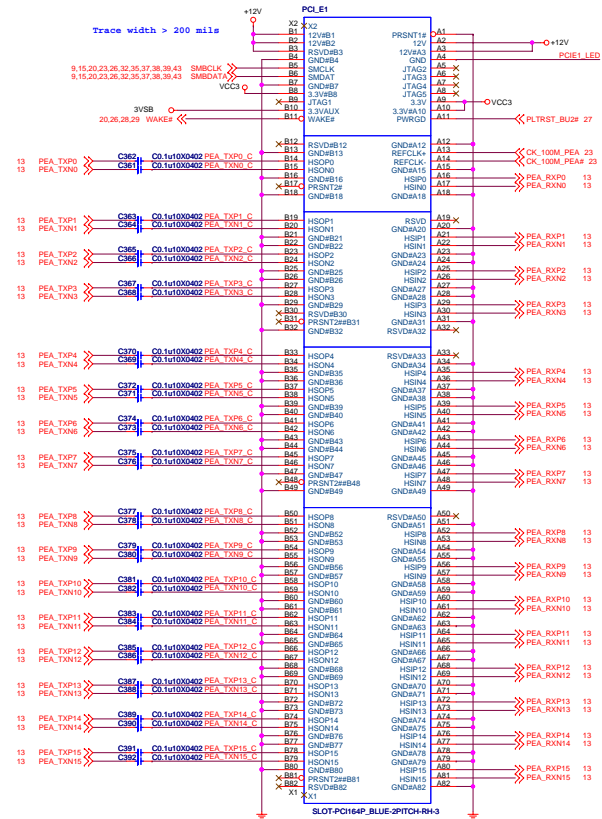
PCI SLOT 1 (PCI VER: 2.2 COMPLY)

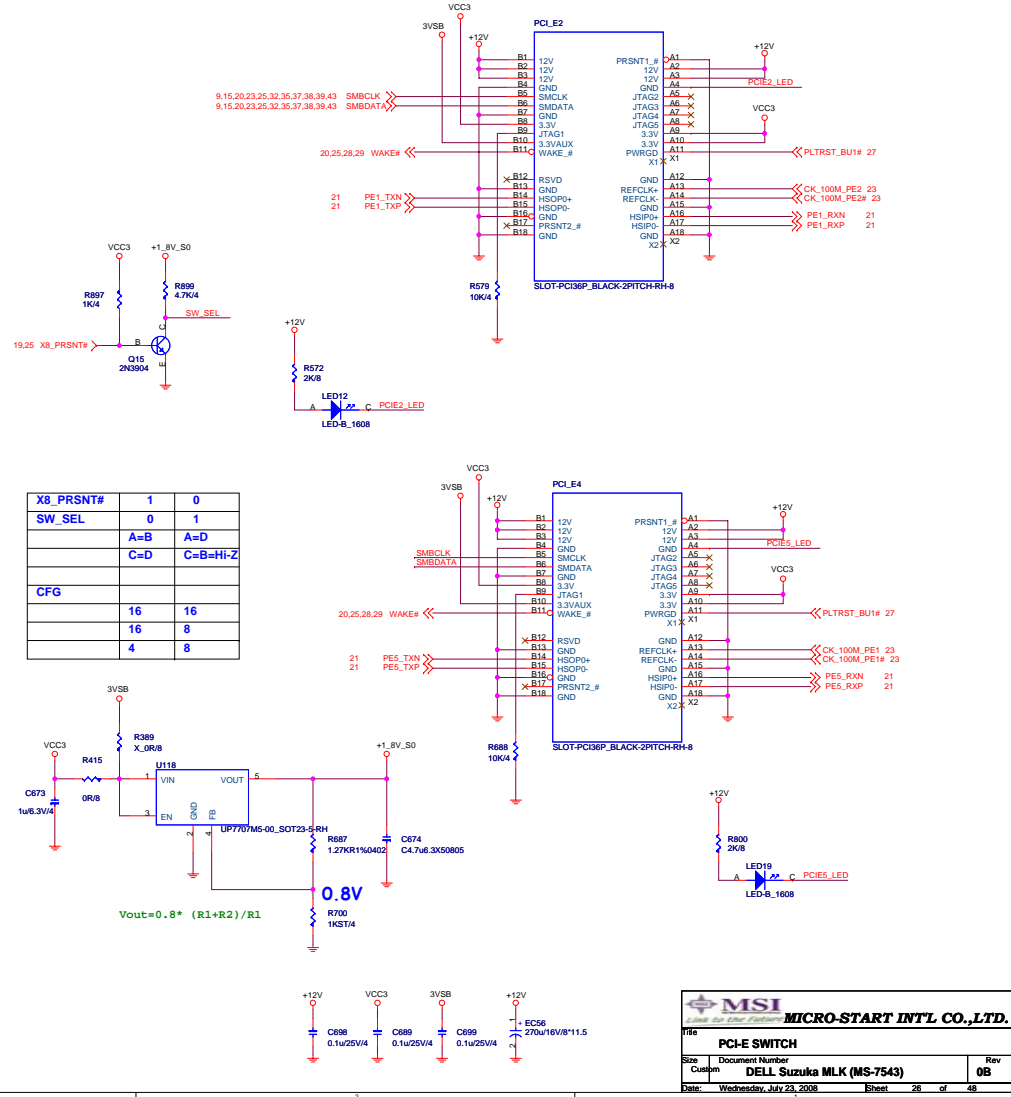


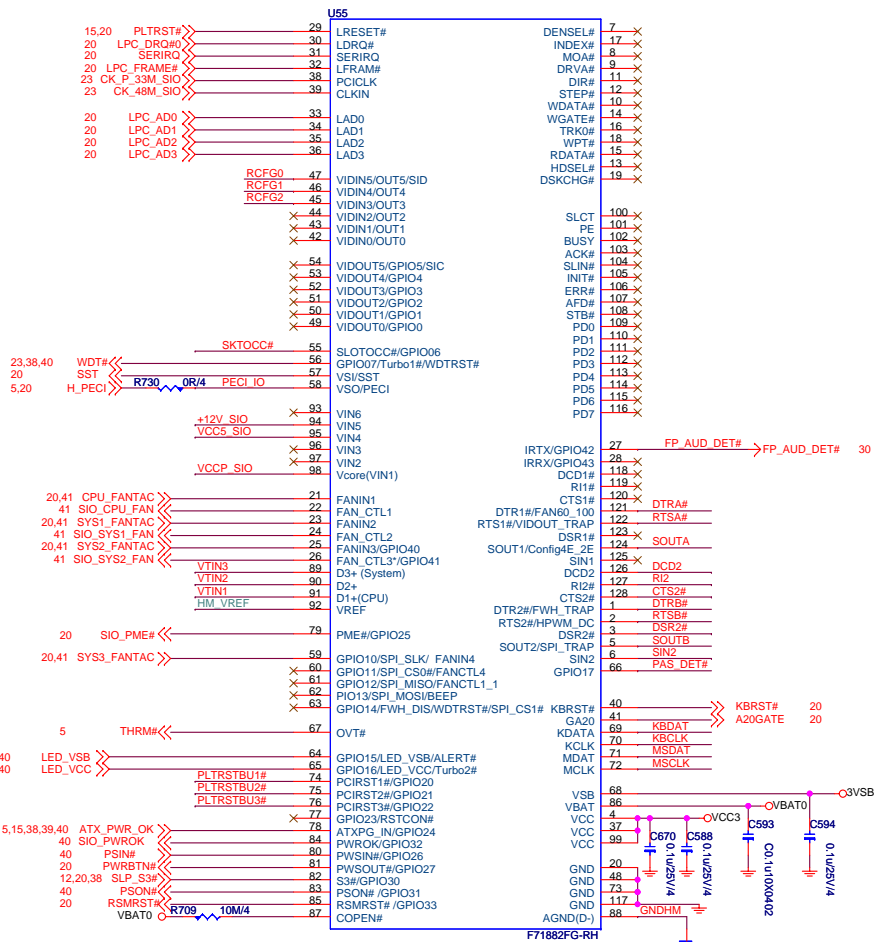
PCI PULL-UP / DOWN RESISTORS



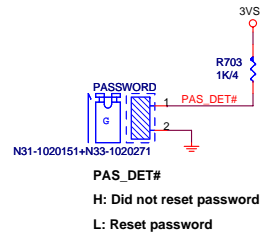
PCI_Express X16 SLOT1,2,3



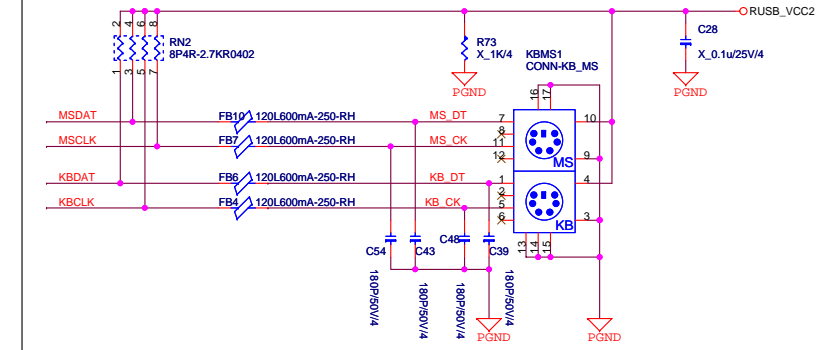




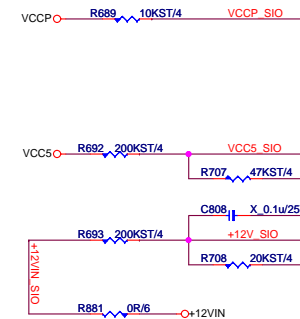
PASSWORD DETECTION



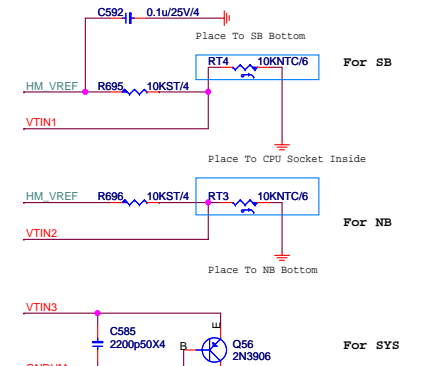
PS2 KEYBOARD & MOUSE CONNECTOR



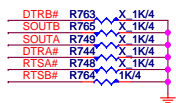
Voltage Sensor



Thermal Resistor



LPC I/O STRAPPING RESISTOR

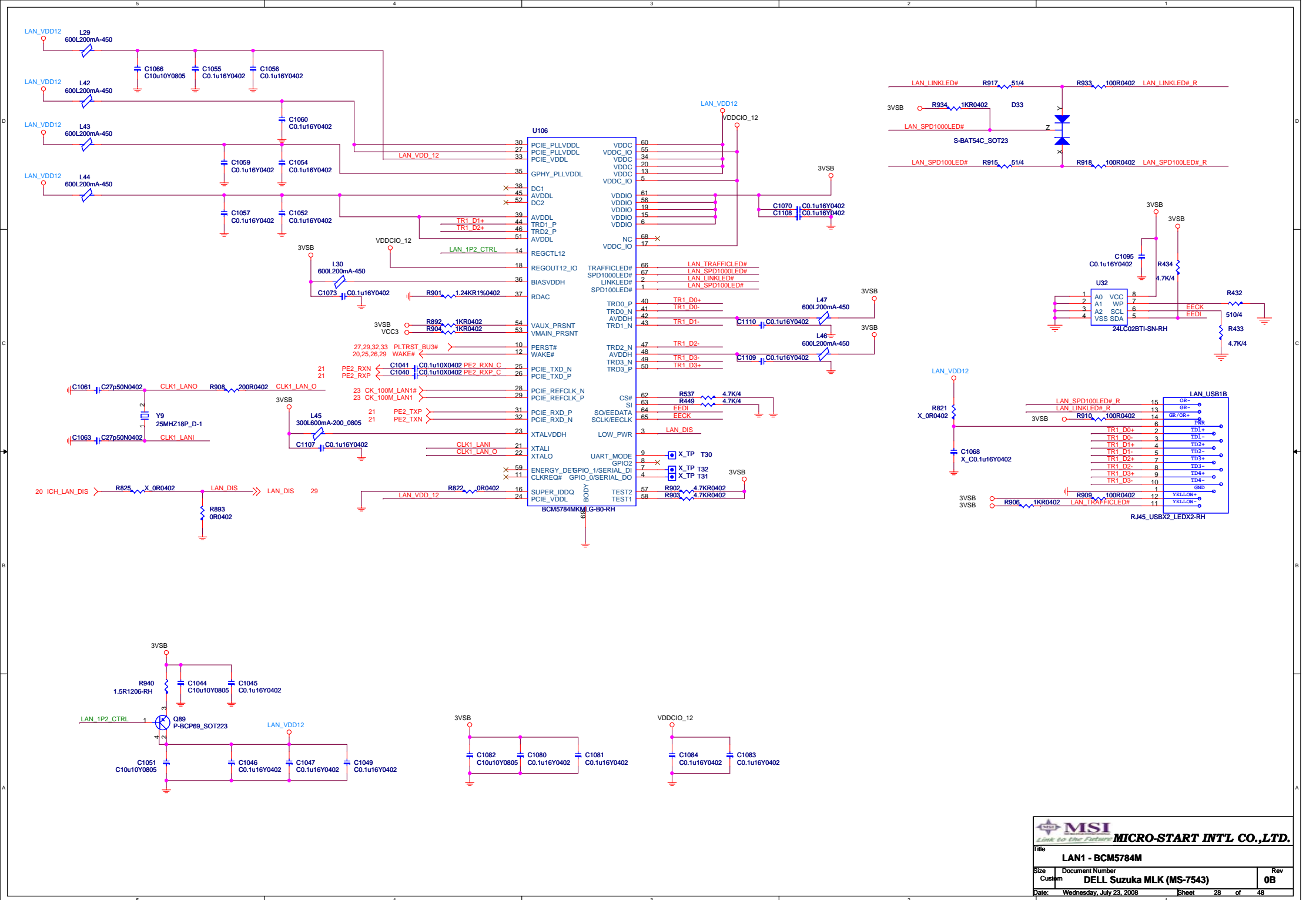


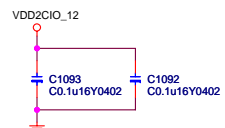
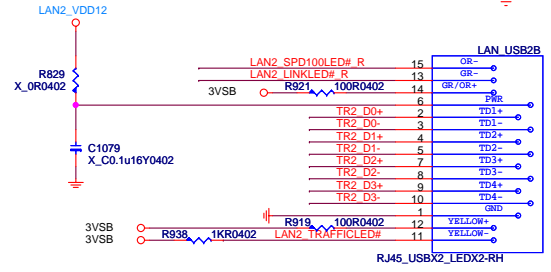
Non used COM2 must pull high

	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT	PIN49-54=GPIO
	PIN42-47=VIDIN	PIN42-47=VIDIN/OUT
SOUTA	4E	2E
DTRB#, SOUTB	SPI_DISABLE	SPI_ENABLE
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%

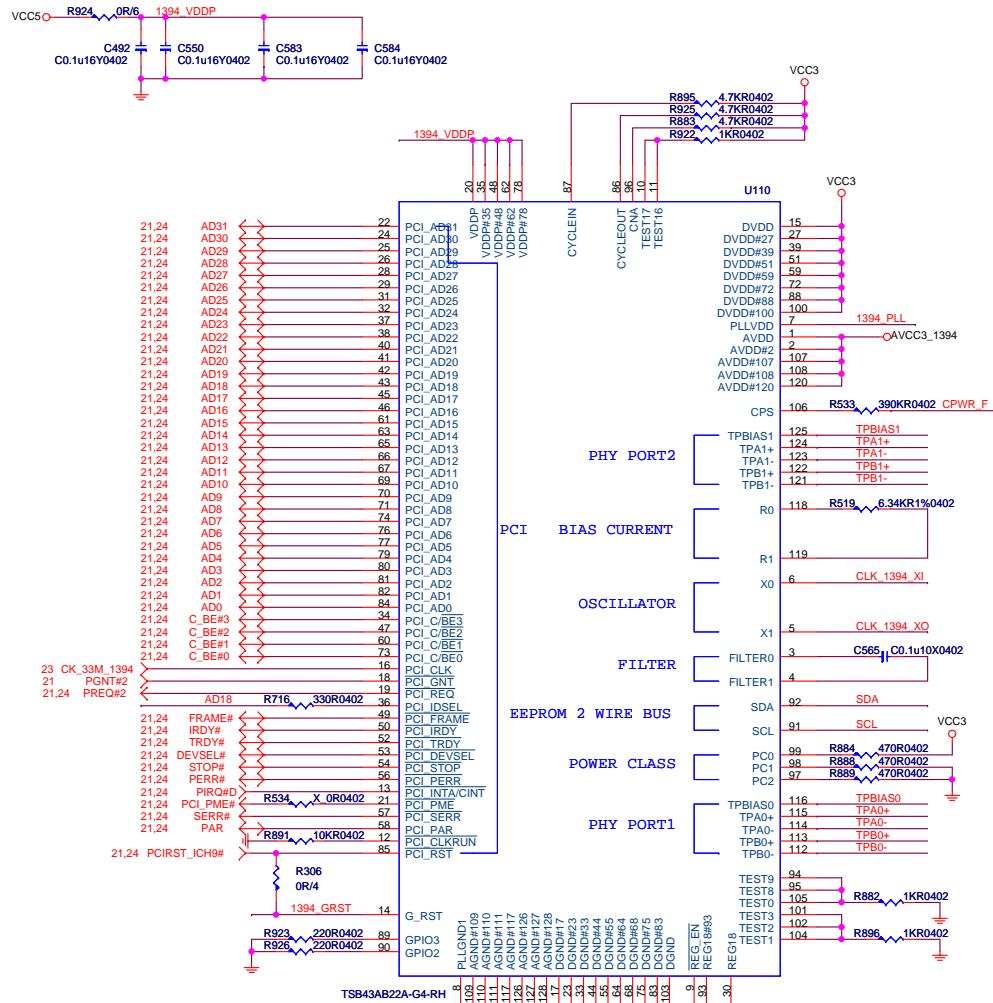
MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

Title	SIO-Fintek F1782F	Rev	0B
Size	Document Number		
Customer	DELL Suzuki MLK (MS-7543)		
Date:	Wednesday, July 23, 2008	Sheet	27 of 48





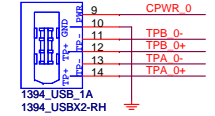
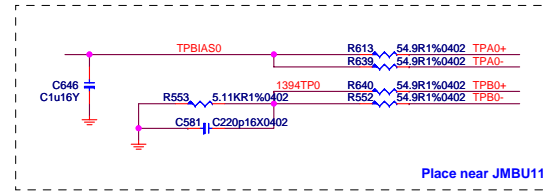
1394 CONTROLLER



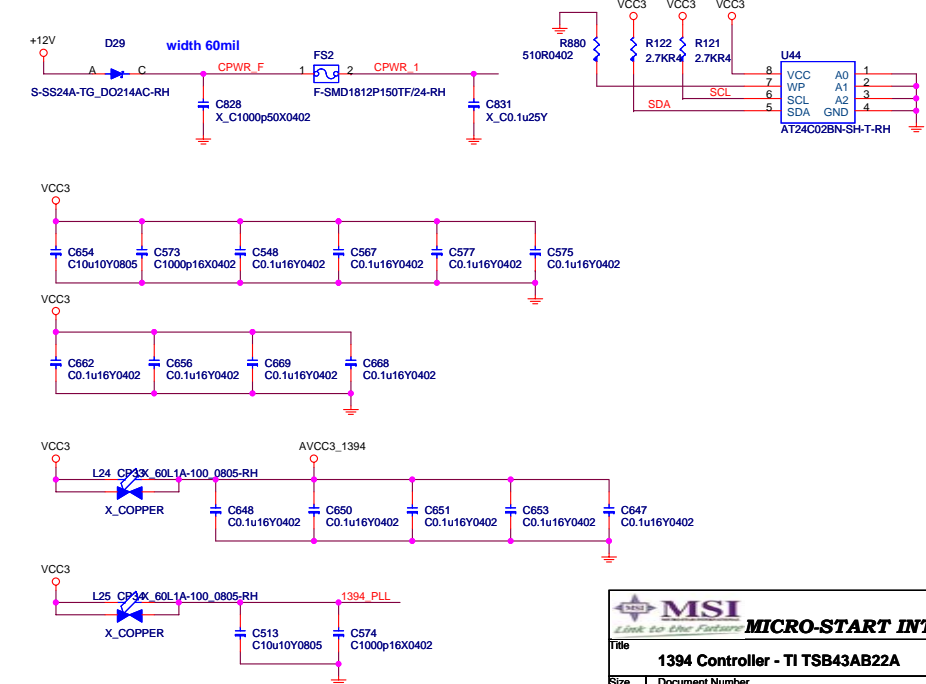
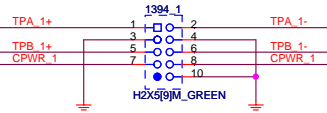
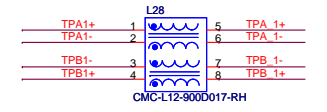
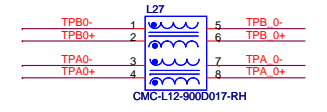
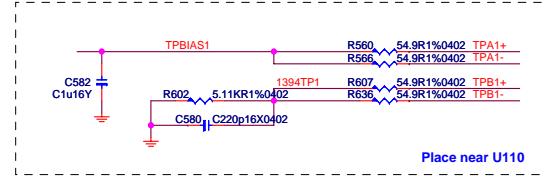
IDSEL = AD18
MASTER = PREQ#2
PGNT#2

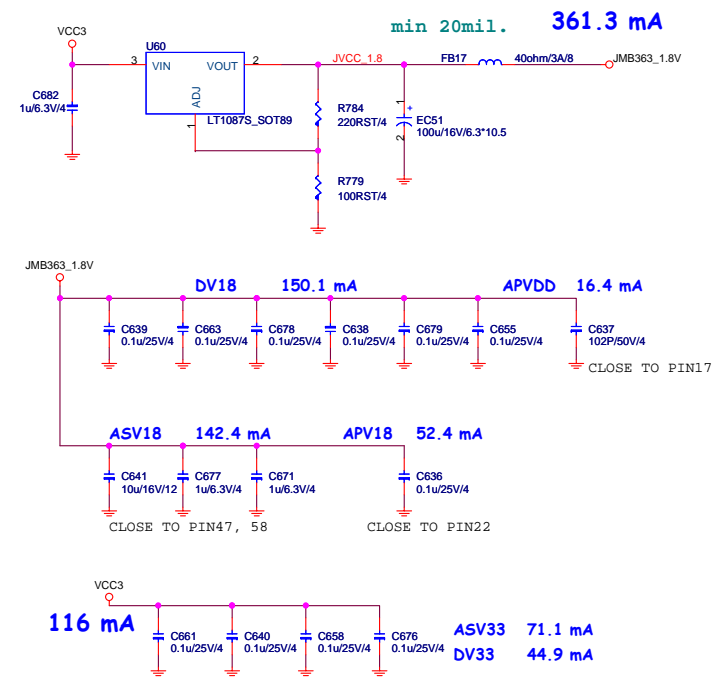
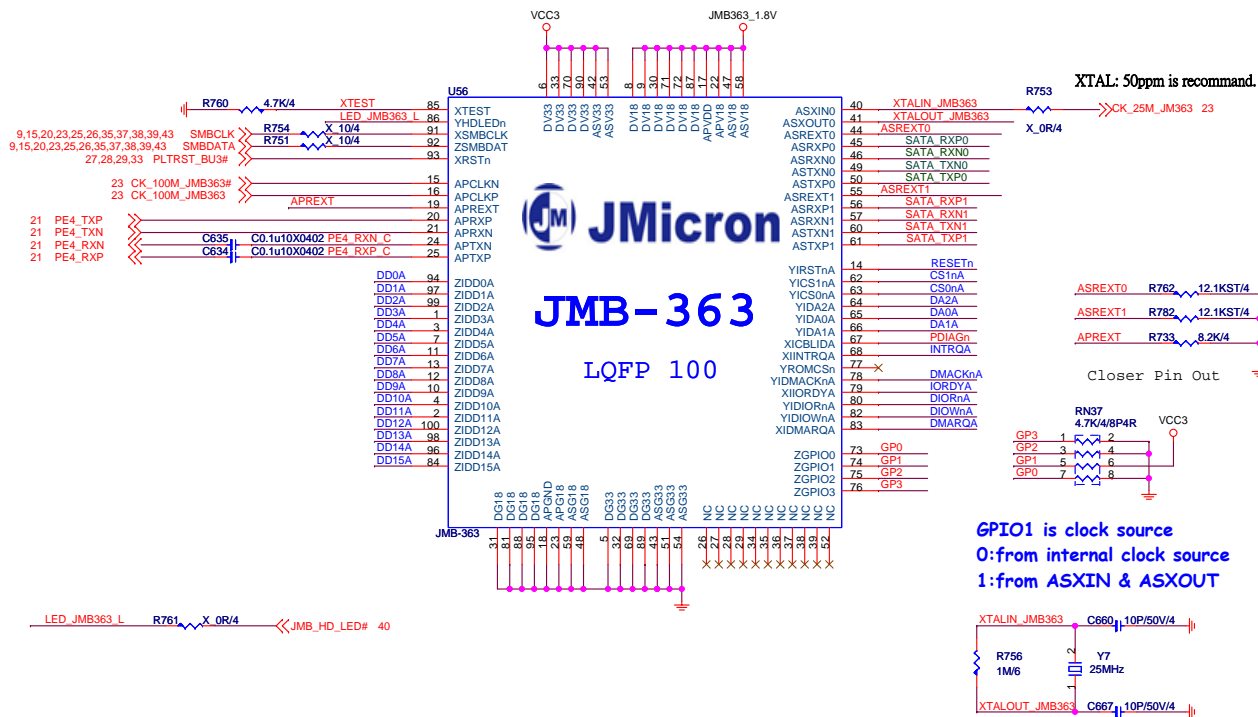


Rear 1394 port

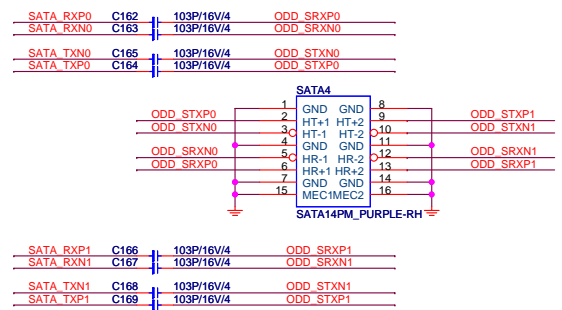


Front 1394 pin header

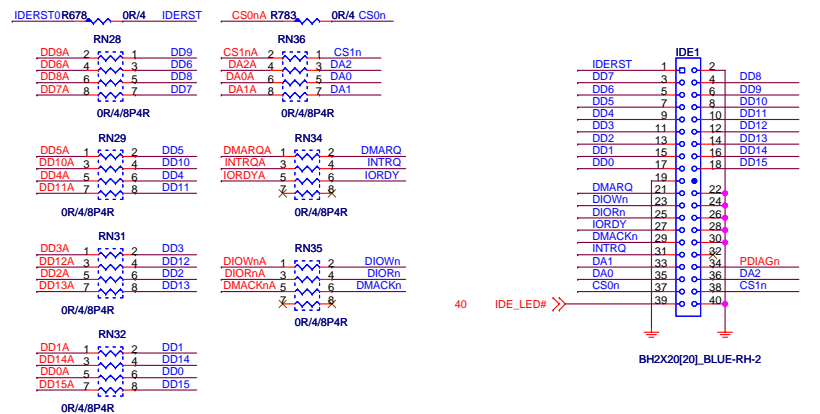
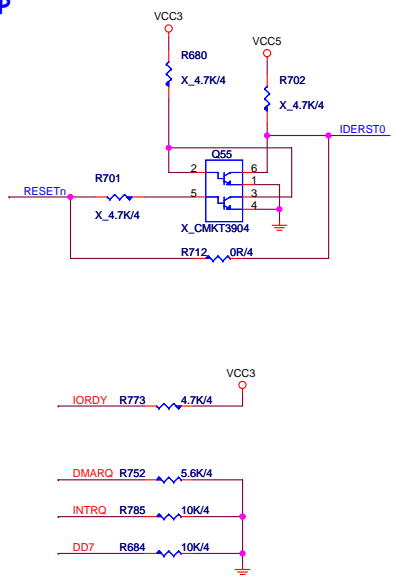




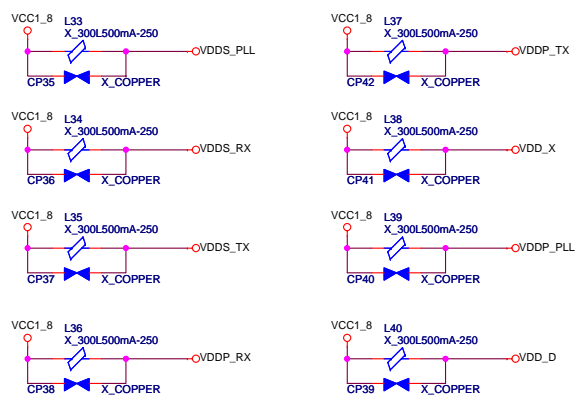
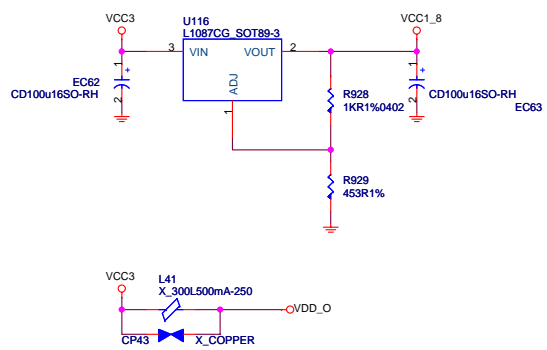
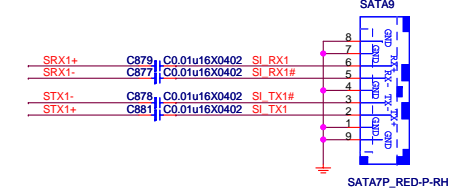
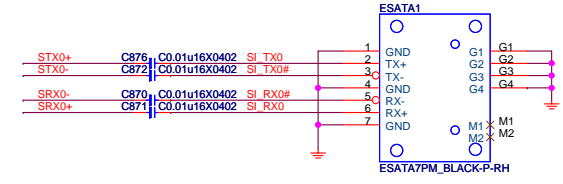
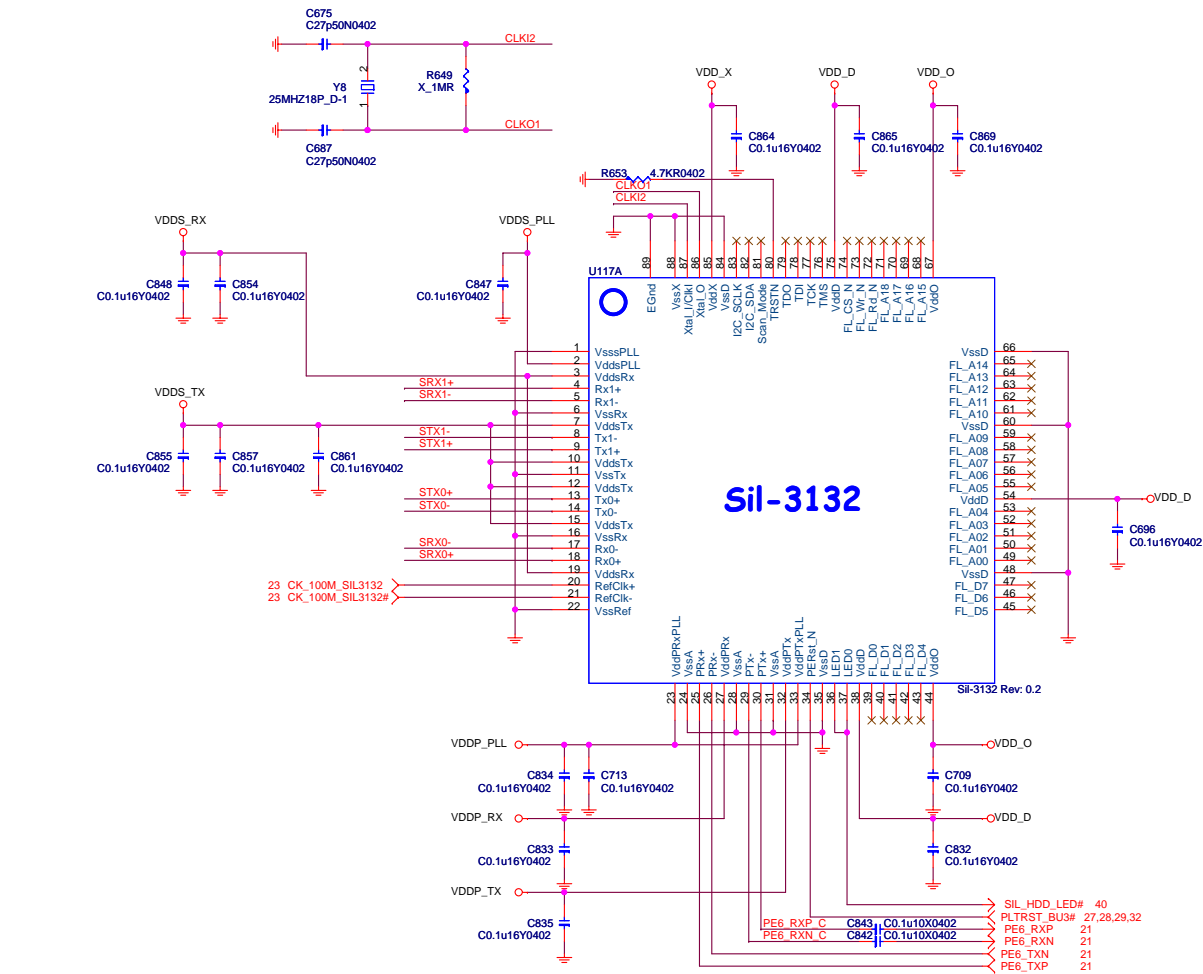
2S



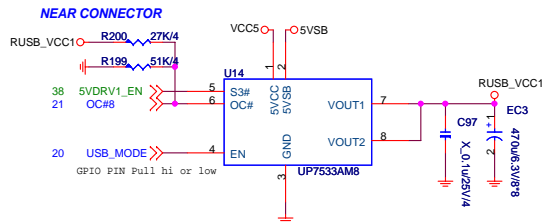
1P



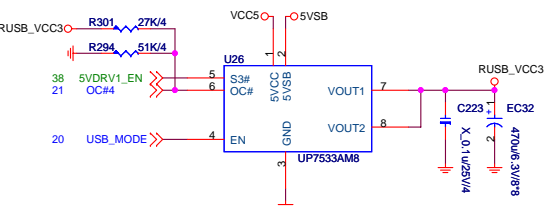
if the length of JMB-363 to IDE connector more than 4inch, that must stuff damping resistor.



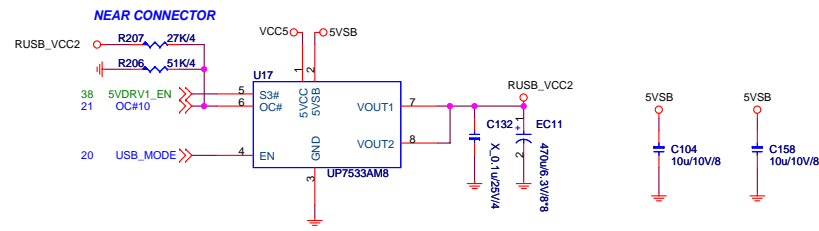
USB POWER FOR PORT 0,1



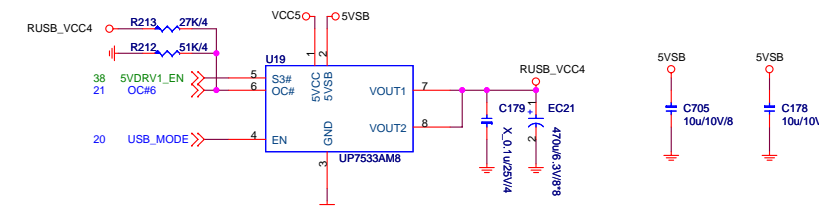
USB POWER FOR PORT 4, 5



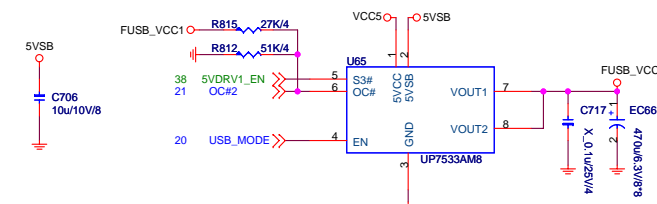
USB POWER FOR PORT 2,3



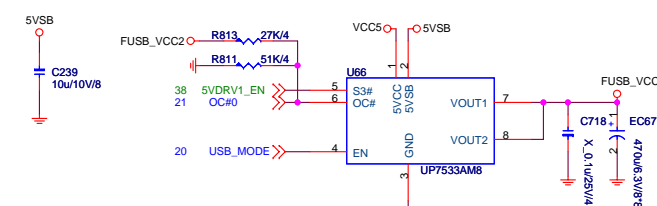
USB POWER FOR PORT 6,7



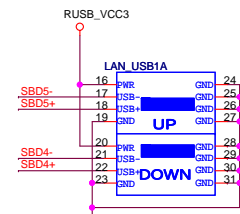
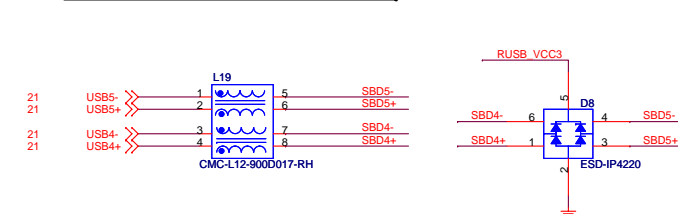
USB POWER FOR PORT 8,9



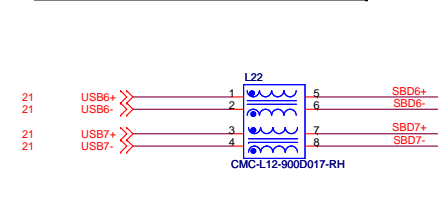
USB POWER FOR PORT 10,11



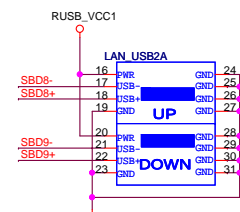
REAR USB PORT 4,5 (With LAN)



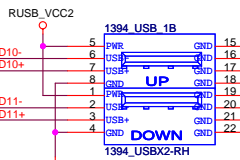
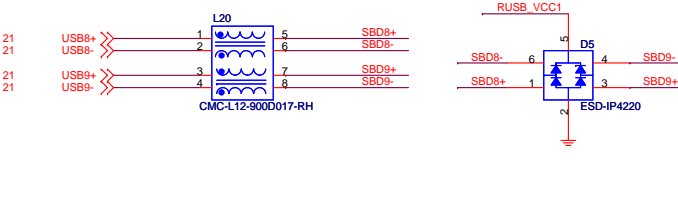
REAR USB PORT 6,7 (With LAN)



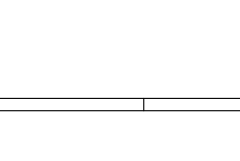
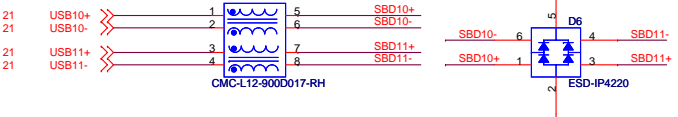
RJ45_USBX2_LEDX2-RH



RJ45_USBX2_LEDX2-RH

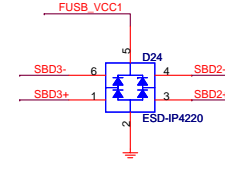
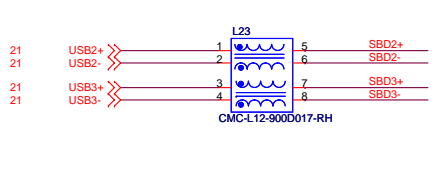


RJ45_USBX2_LEDX2-RH

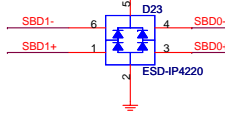
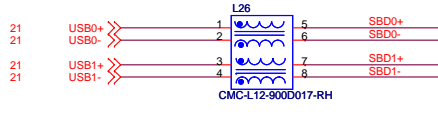


RJ45_USBX2_LEDX2-RH

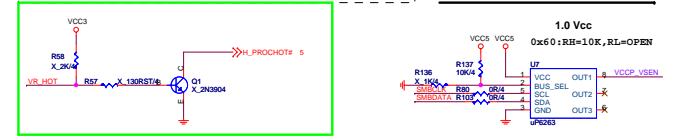
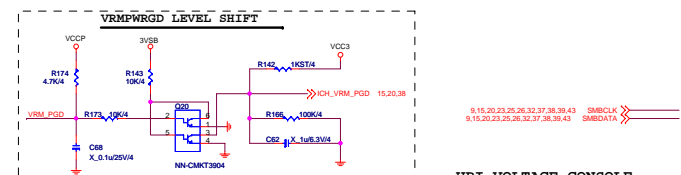
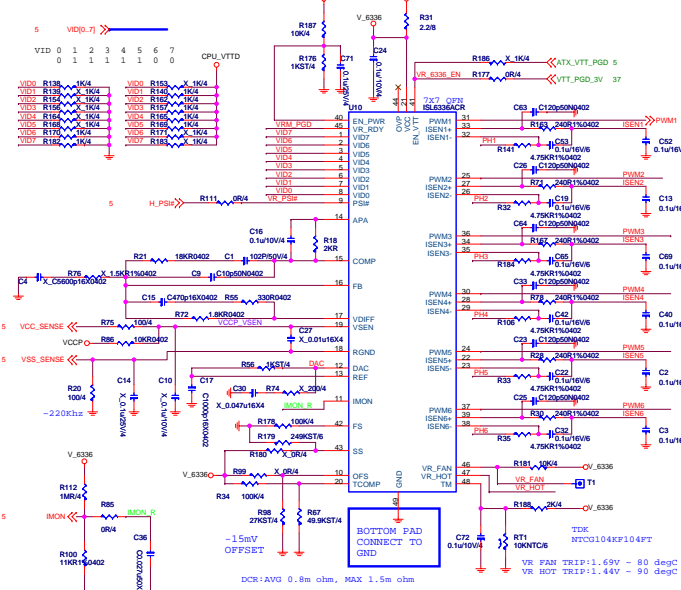
FRONT USB PORT 8,9



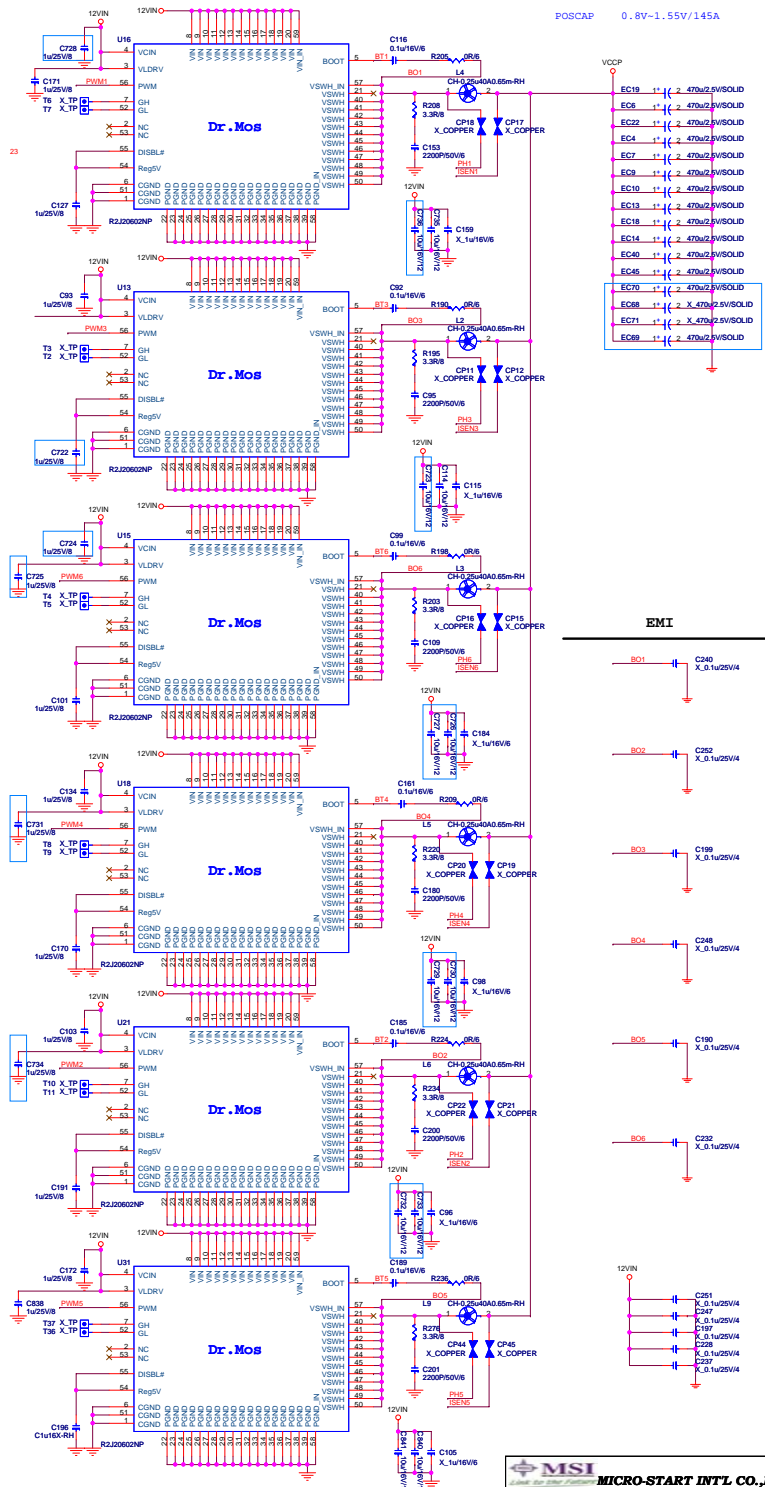
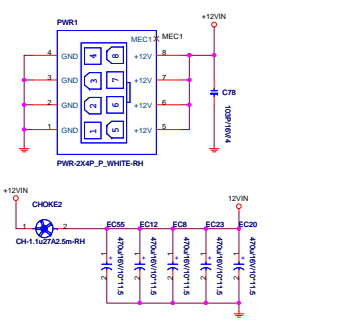
FRONT USB PORT 10,11




ISL6336CR VRD11.1 POWER CKT

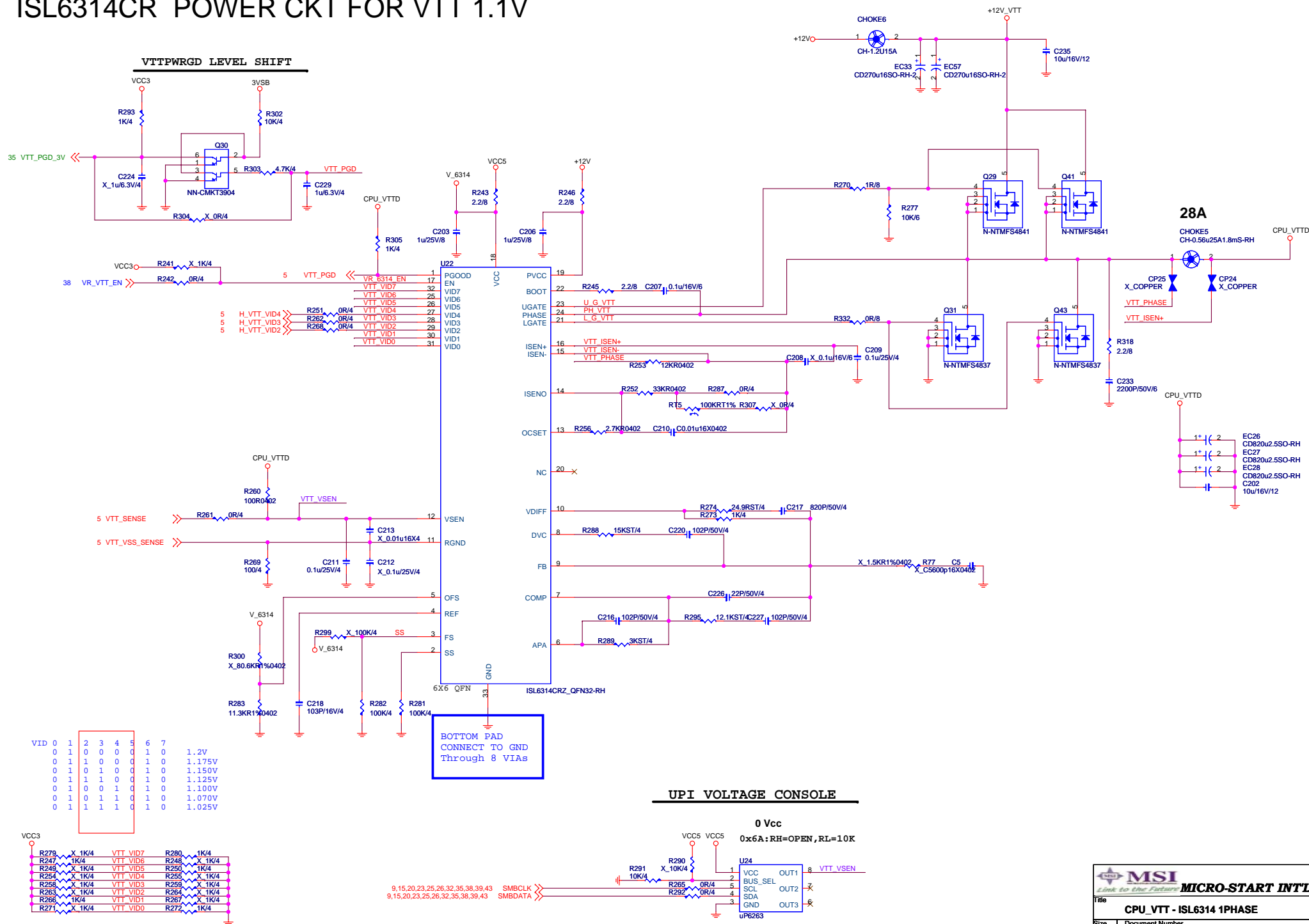


CPU +12VIN POWER CONN.

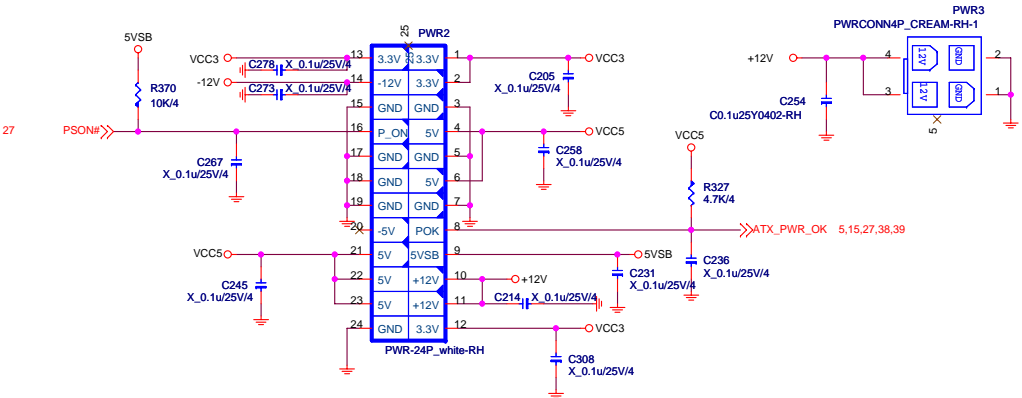


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File							
VRD11.1 - ISL6336 6-PHASE							
Size Custom		Document Number DELL Suzuki MLK (MS-7543)				Rev 0B	
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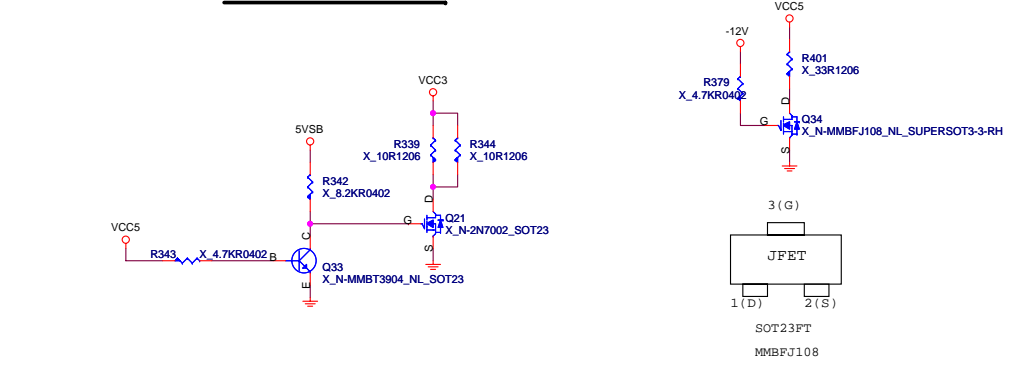
ISL6314CR POWER CKT FOR VTT 1.1V



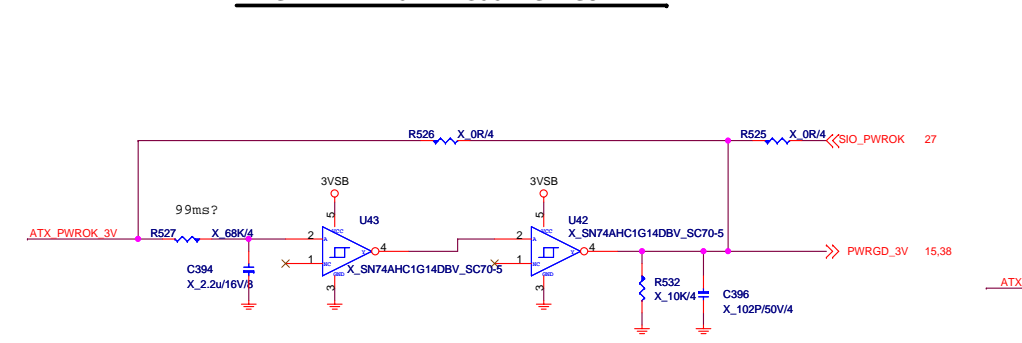
ATX POWER CONNECTOR



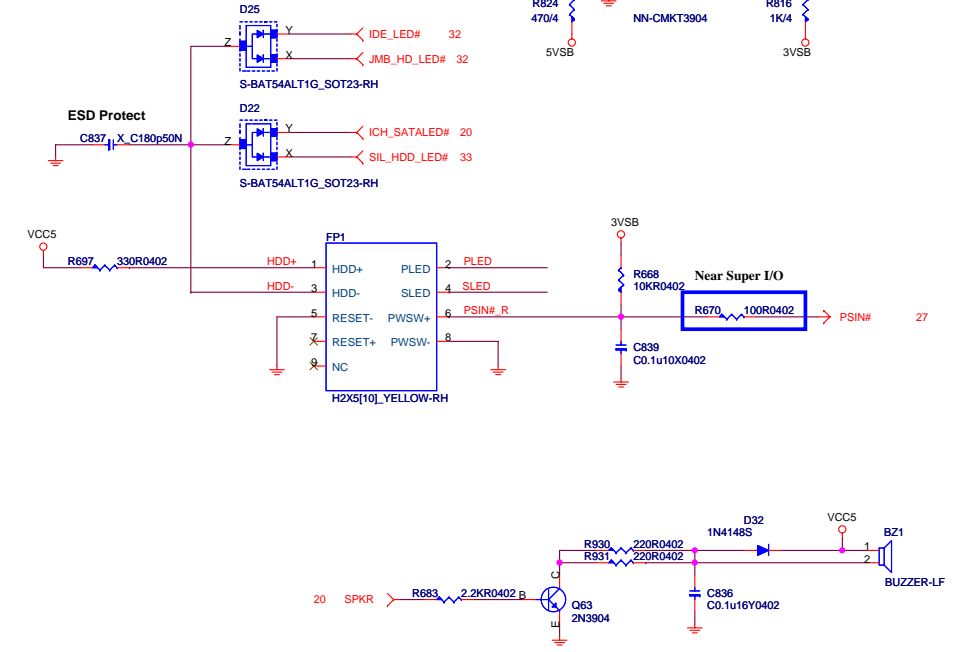
Minimum Load



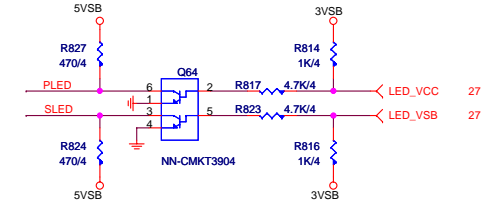
CHIPSET POWER GOOD CIRCUIT



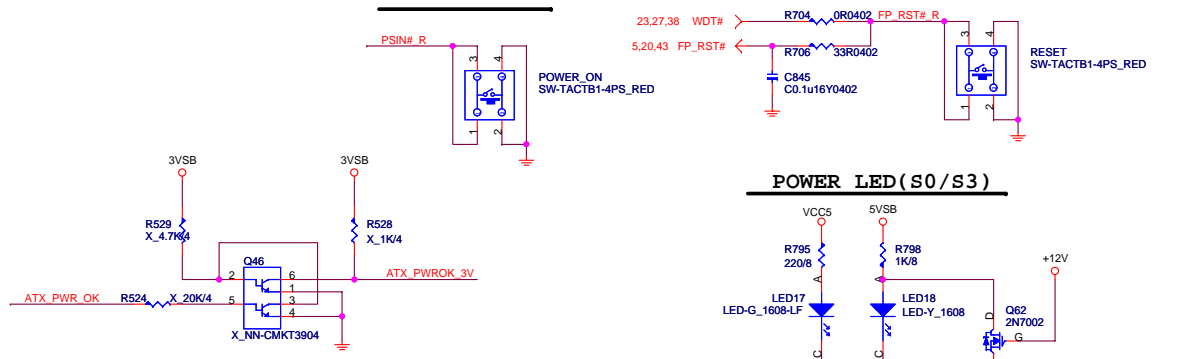
FRONT PANNEL



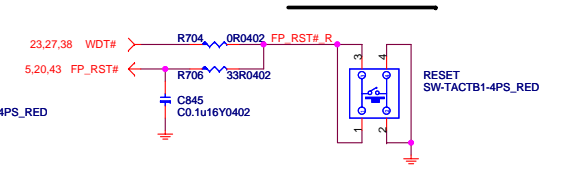
LED (By Fintek 71882)



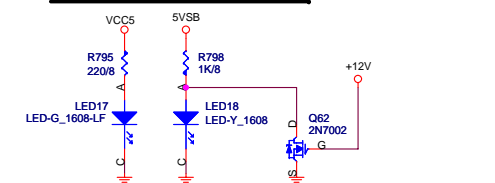
POWER ON BUTTON



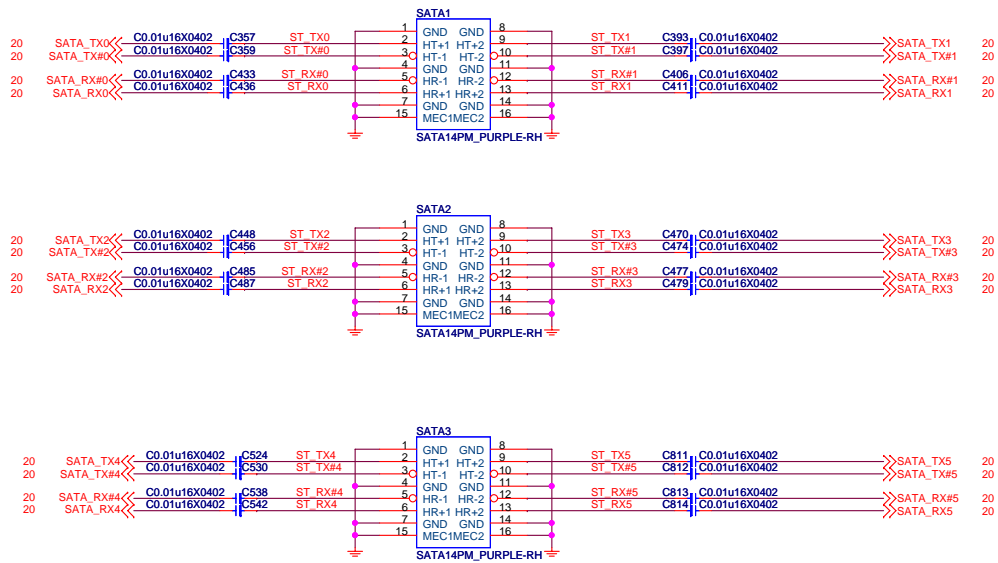
RESET BUTTON



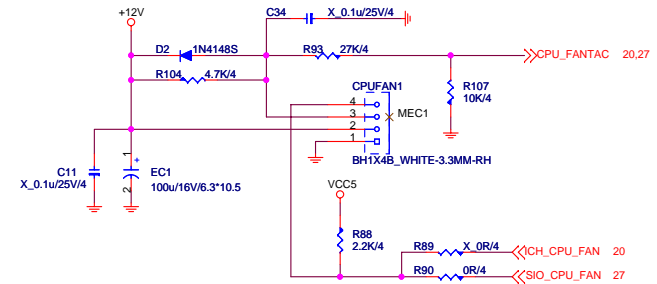
POWER LED (S0/S3)



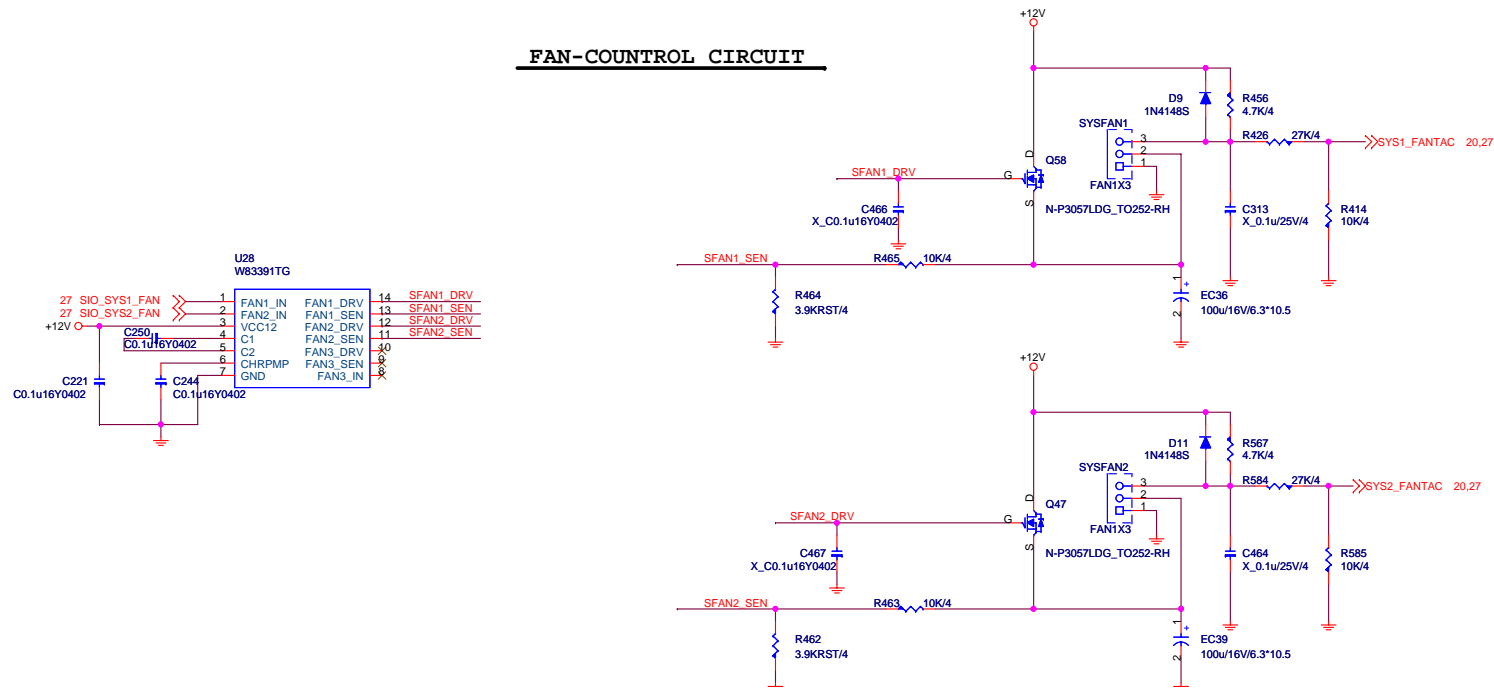
SATA-II Connector



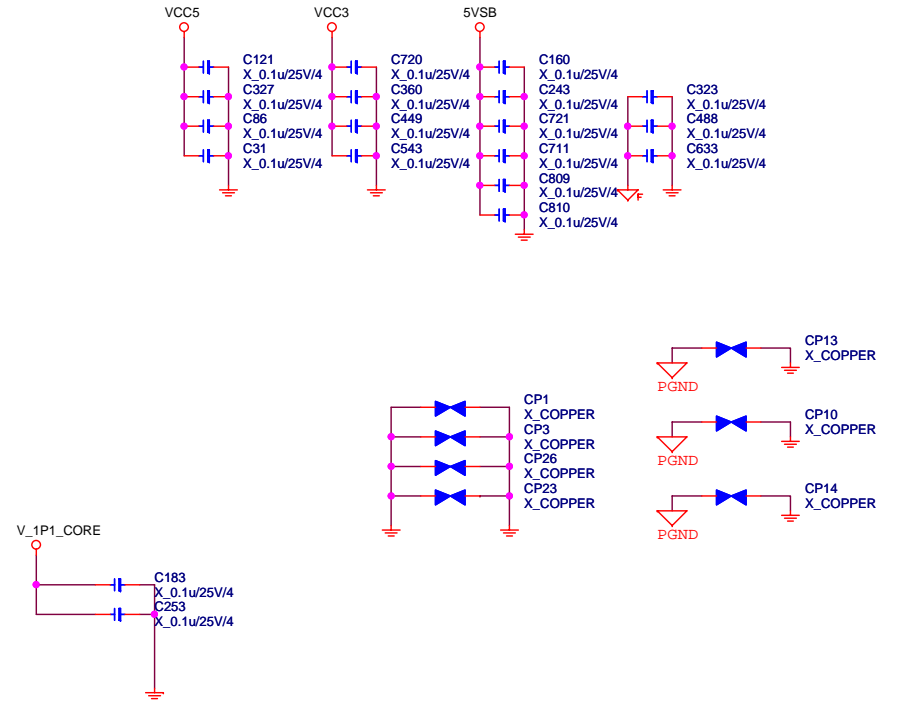
CPU FAN



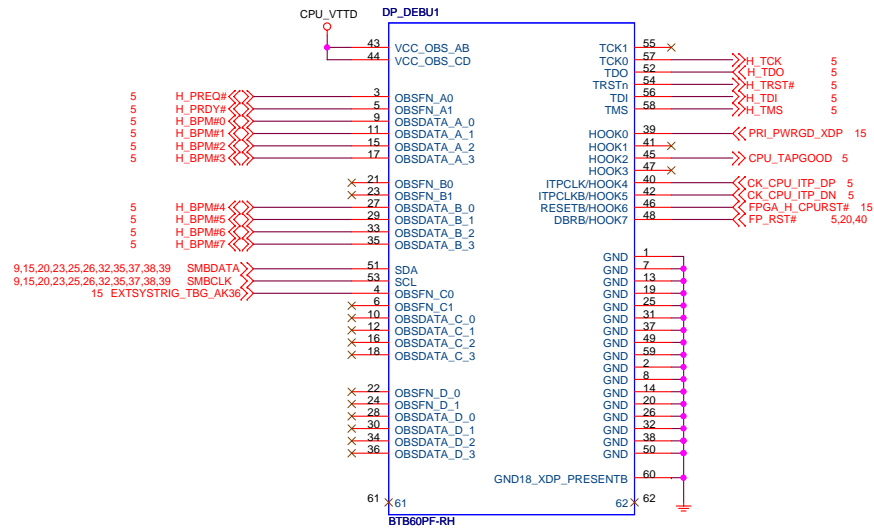
FAN-COUNTROL CIRCUIT



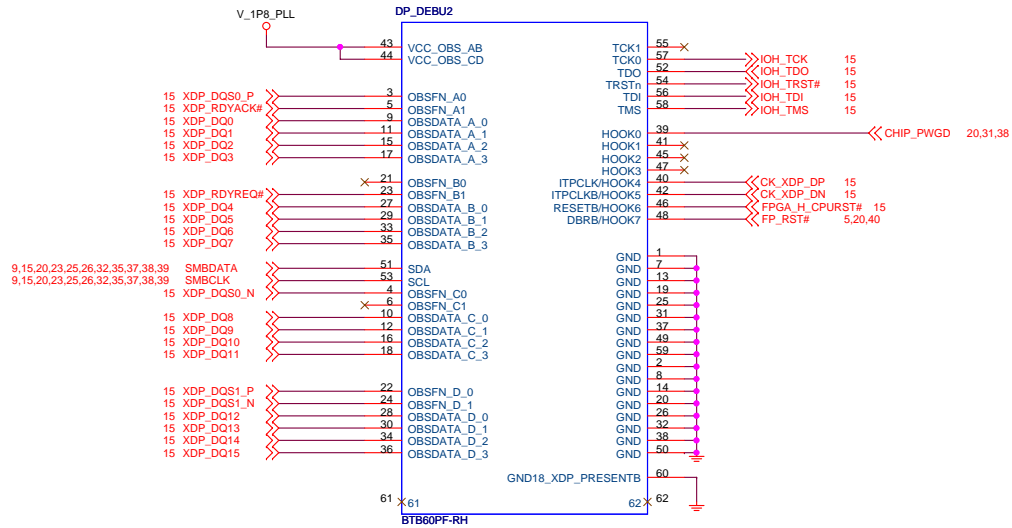
EMI CAP



Reserve debug port 5020



Reserve debug port 5020





PP0-075430B-B32
PP0-075430B-T53



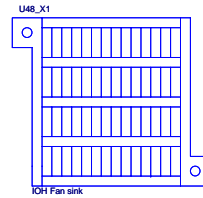
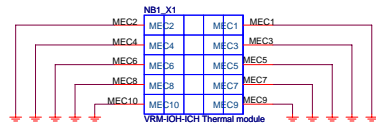
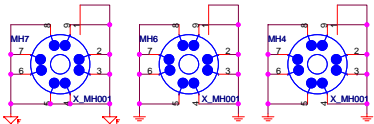
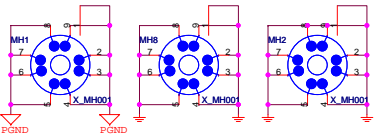
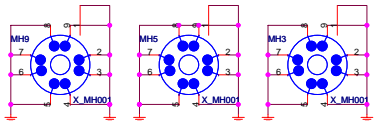
Optical Fiducial Marks-120



Optical Fiducial Marks-100



Mounting Holes

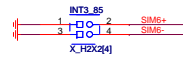


Simulation

4/8 95 ohm

5/5 85 ohm

5/7 85 ohm



Manual Parts

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Custom	DELL Suzuka MLK (MS-7543)	0B
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